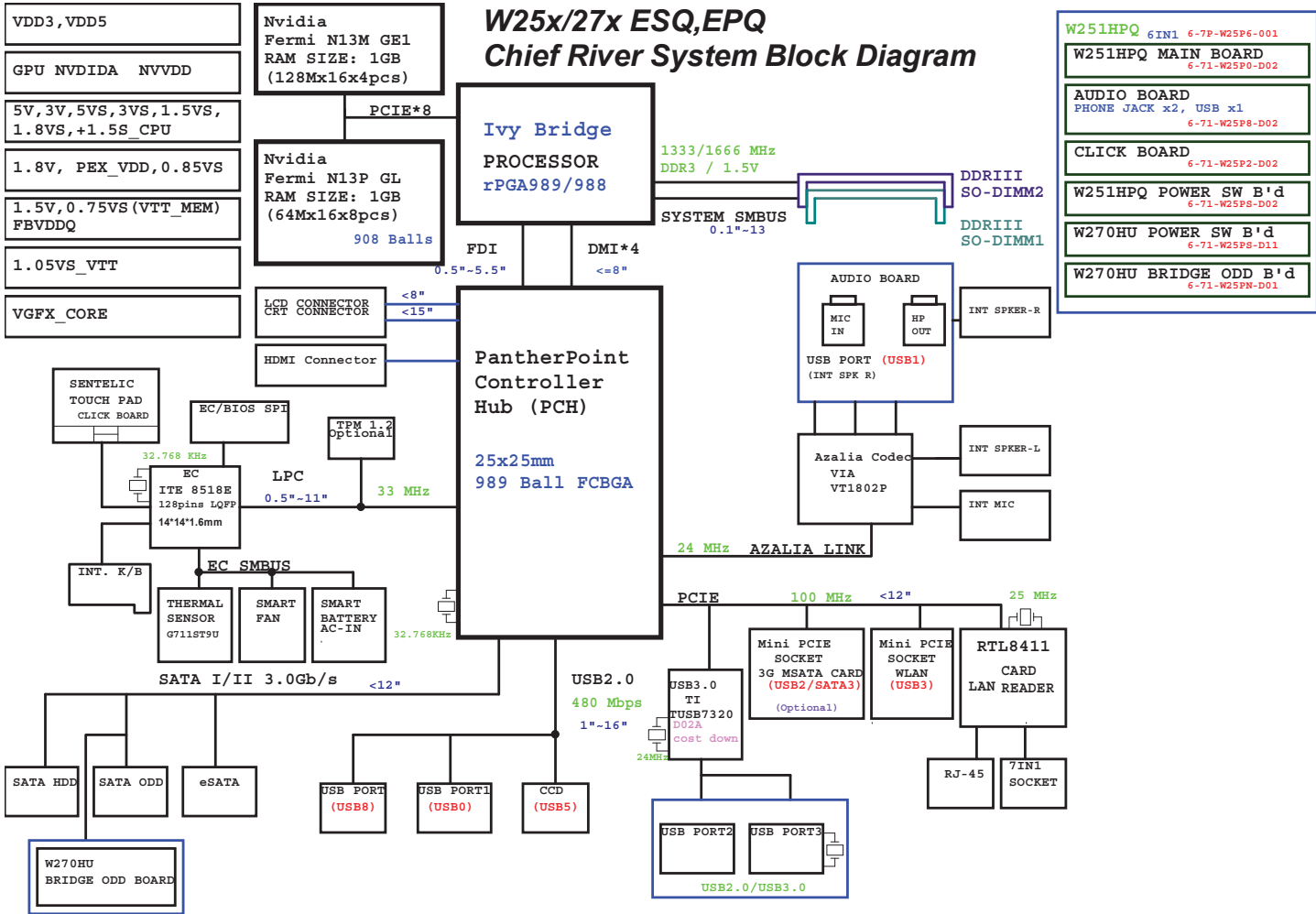


System Block Diagram

Sheet 1 of 50
System Block
Diagram



Processor 1/7-DMI, FDI, PEG

Ivy Bridge Processor 1/7 (DMI,PEG,FDI)

Ivy Bridge Quad Core 55W

Ivy Bridge Dual Core 35W

Ivy Bridge LV/ULV 25/17W

2012 Ivy Bridge Socket compatible with Sandy Bridge.

2012 Ivy Bridge Same TDP as Sandy Bridge.

2012 Ivy DDR3-1600 and DDR3L-1333 Support.

2012 Ivy PCIe*Gen3.0(PEGX16).

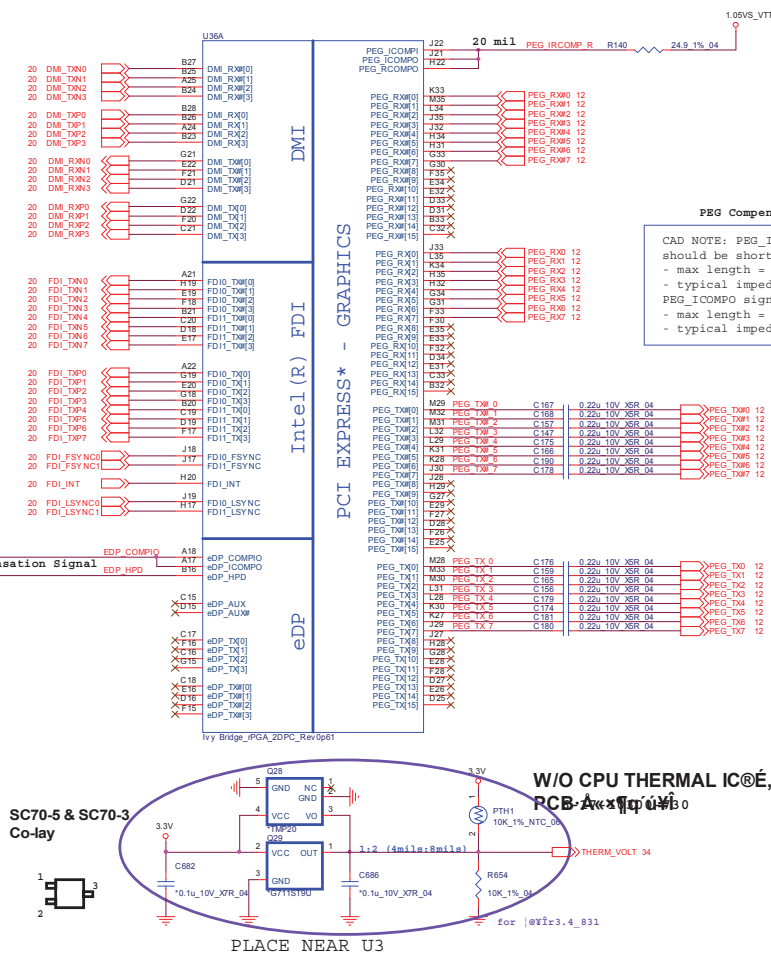
2012 Ivy DX11 Support, 3 Simultaneous Displays.

CAD NOTE: DP_COMPIO and ICOMPO signals should be shorted near balls and routed with - typical impedance < 25 mohms

EDP HPD Function Disable
EDP_HPDPull-up10K- DISABLED HPD

CPU

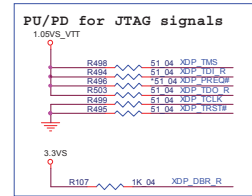
H8 H8_0D4_4 H8_0D4_4 H8_0D4_4



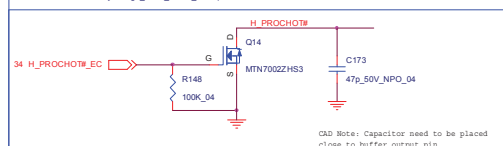
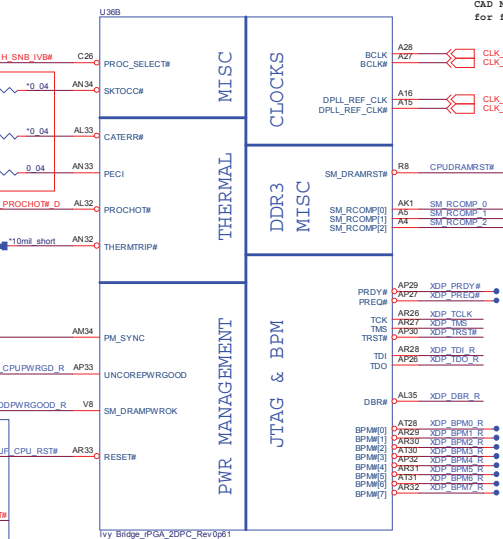
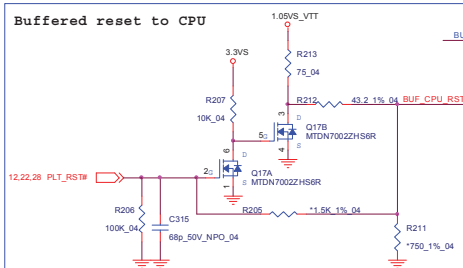
Schematic Diagrams

Processor 2/7- CLK, MISC

Ivy Bridge Processor 2/7 (CLK,MISC,JTAG)



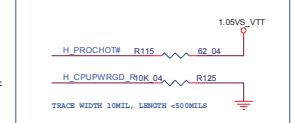
If PROCHOT# is not used, then it must be terminated with a 56- Ω \pm 5% pull-up resistor to 1.05VS_VTT.



CAD Note: Use pad sharing method for following clock resistor placement

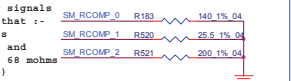


Processor Pullups/Pull downs

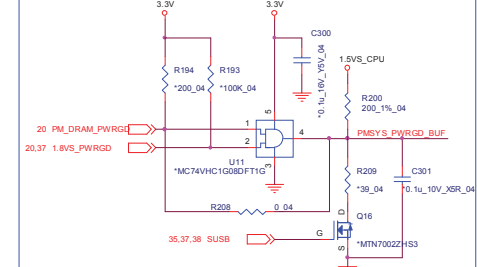


DDR3 Compensation Signals

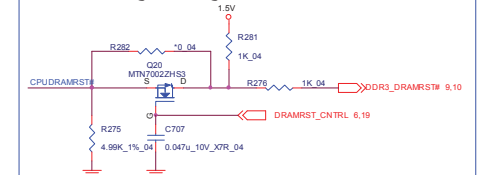
CAD NOTE: All DDR_COMP signals should be routed such that:-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms (worst case resistance)



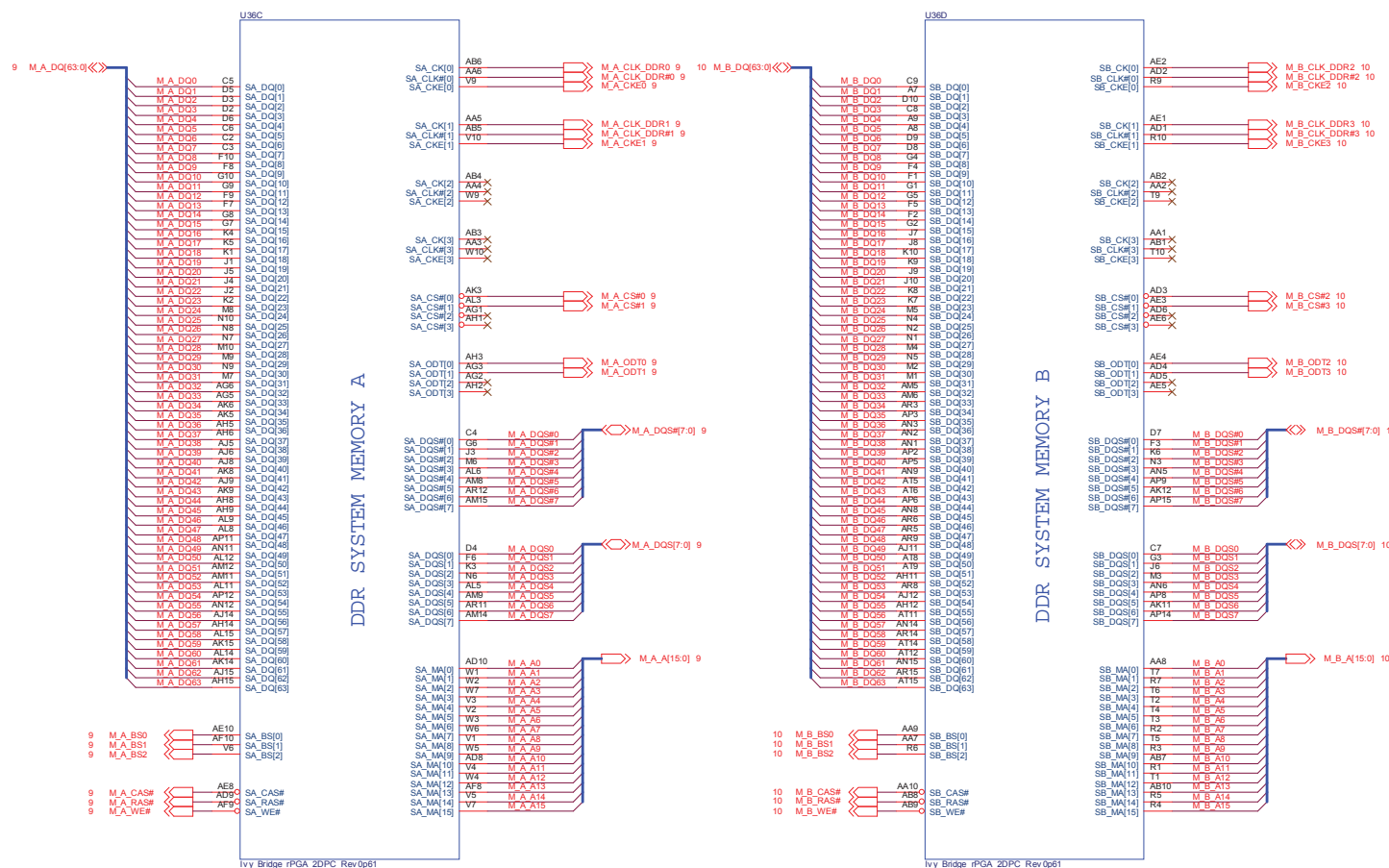
S3 circuit:- DRAM PWR GOOD logic



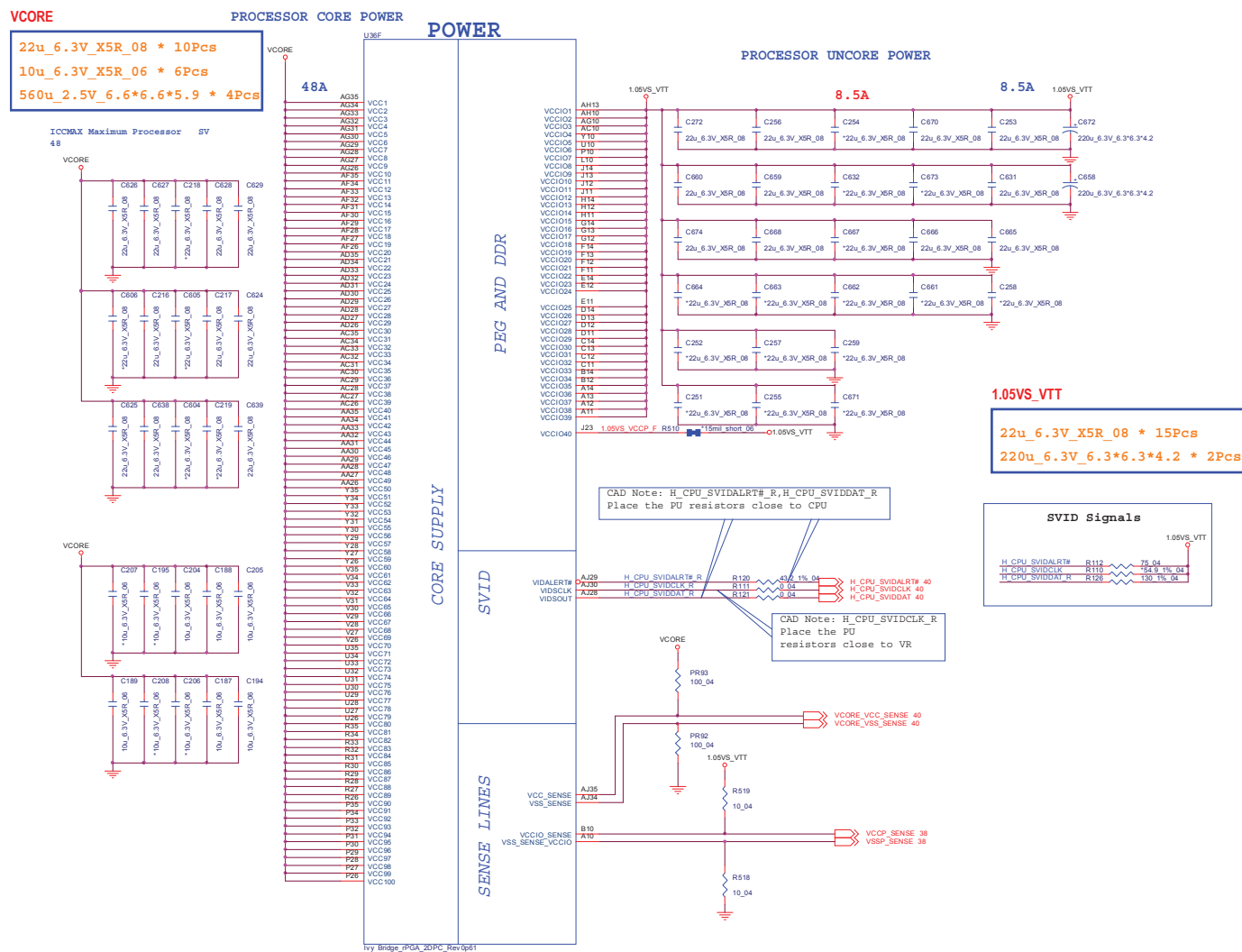
S3 circuit:- DRAM RST# to memory should be high during S3



Ivy Bridge Processor 3/7 (DDR3)



Ivy Bridge Processor 4/7 (POWER)



Ivy Bridge Processor 5/7 (GRAPHICS POWER)



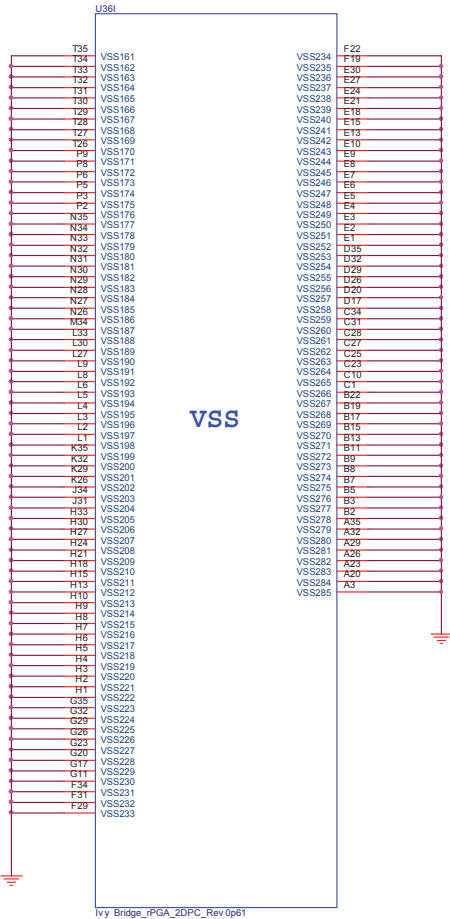
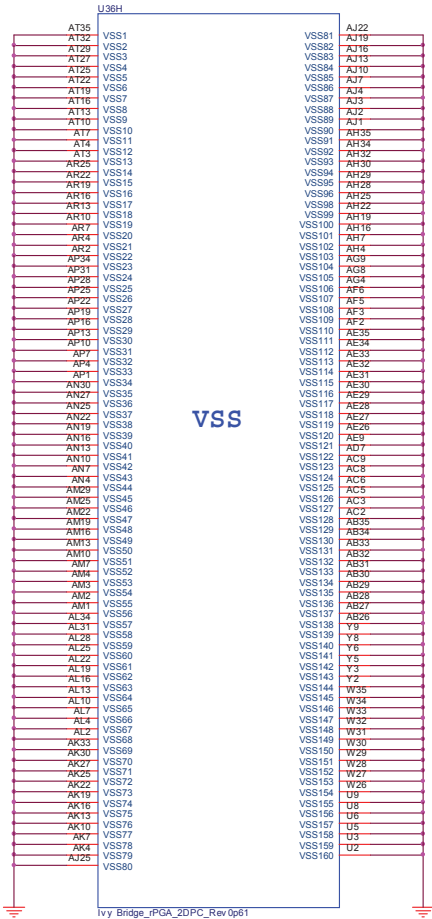
Schematic Diagrams

Processor 6/7- GND

Ivy Bridge Processor 6/7 (GND)

CAD Note: 0 ohm resistor
should be placed close
to CPU

Sheet 7 of 50
Processor 6/7- GND



Processor 7/7- RSVD

Ivy Bridge Processor 7/7 (RESERVED)

CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed

CFG2 R497 *1K.04

Display Port Presence Strap

CFG4 1: (Default) Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 R124 *1K.04

PCIe Port Bifurcation Straps

CFG[6:5] 11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

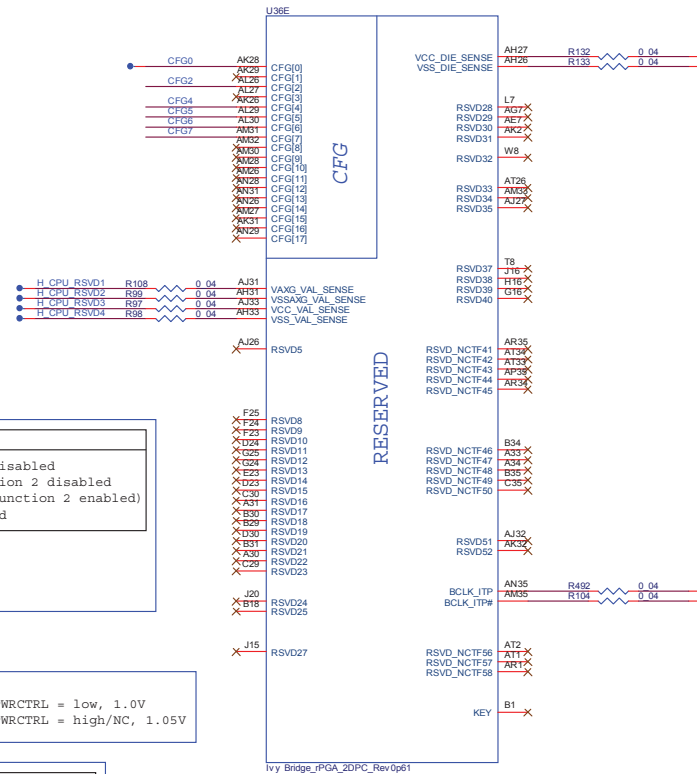
CFG5 R114 *1K.04 C100889
CFG6 R105 *1K.04

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

PEG DEFER TRAINING

CFG7 1: (Default) PEG Train immediately following xRES# de assertion
0: PEG Wait for BIOS for training

CFG7 R113 *1K.04



Sheet 8 of 50
Processor 7/7-
RSVD

B.Schematic Diagrams

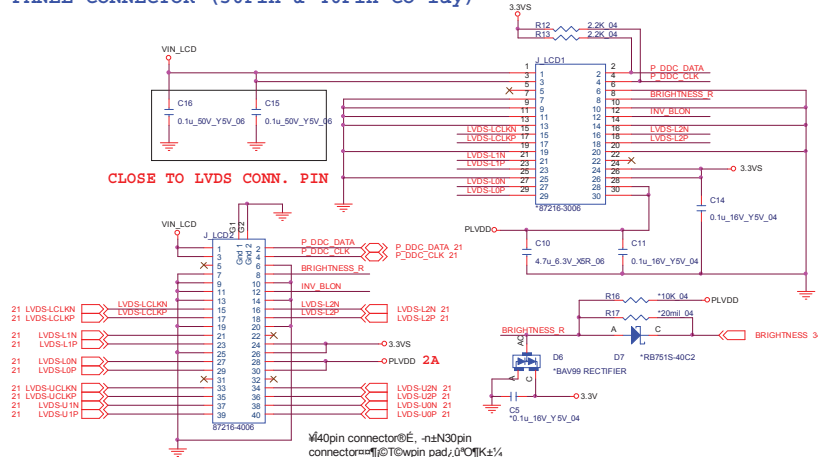
SO-DIMM A



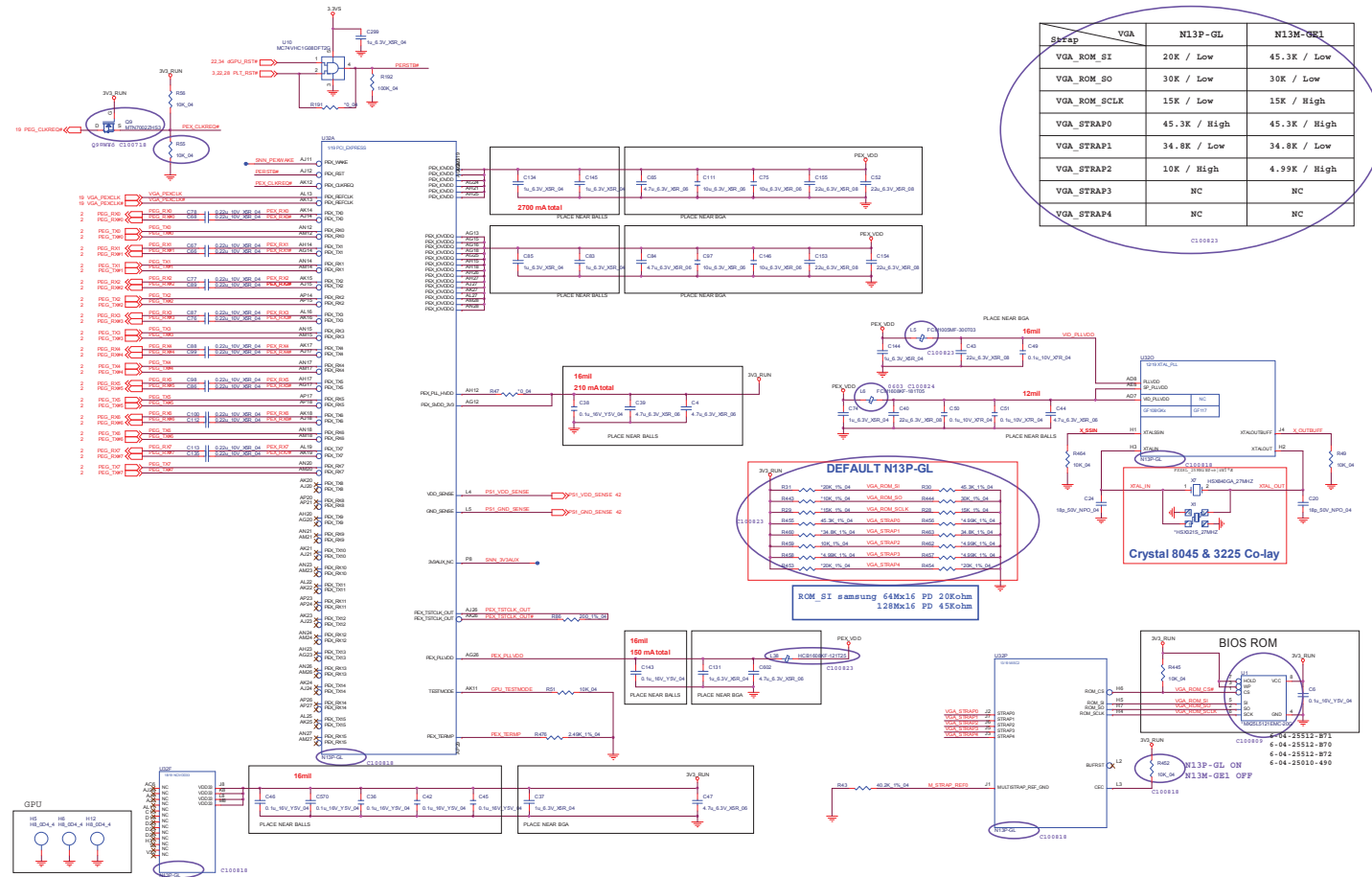
SO-DIMM B



Sheet 11 of 50
PANEL, INVERTER,
CRT

[illegible][illegible]

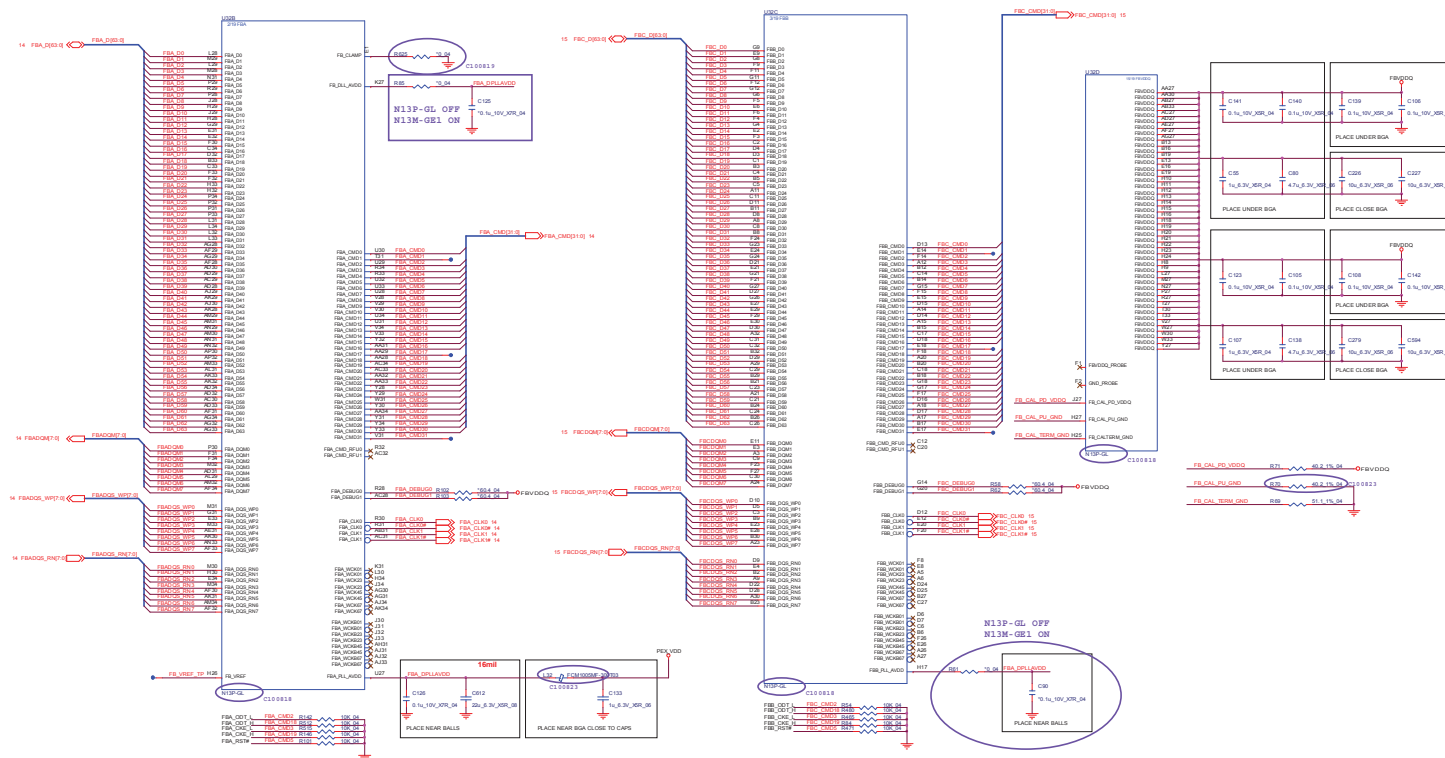
VGA PCI-E Interface



Sheet 12 of 50
VGA PCI-E
Interface

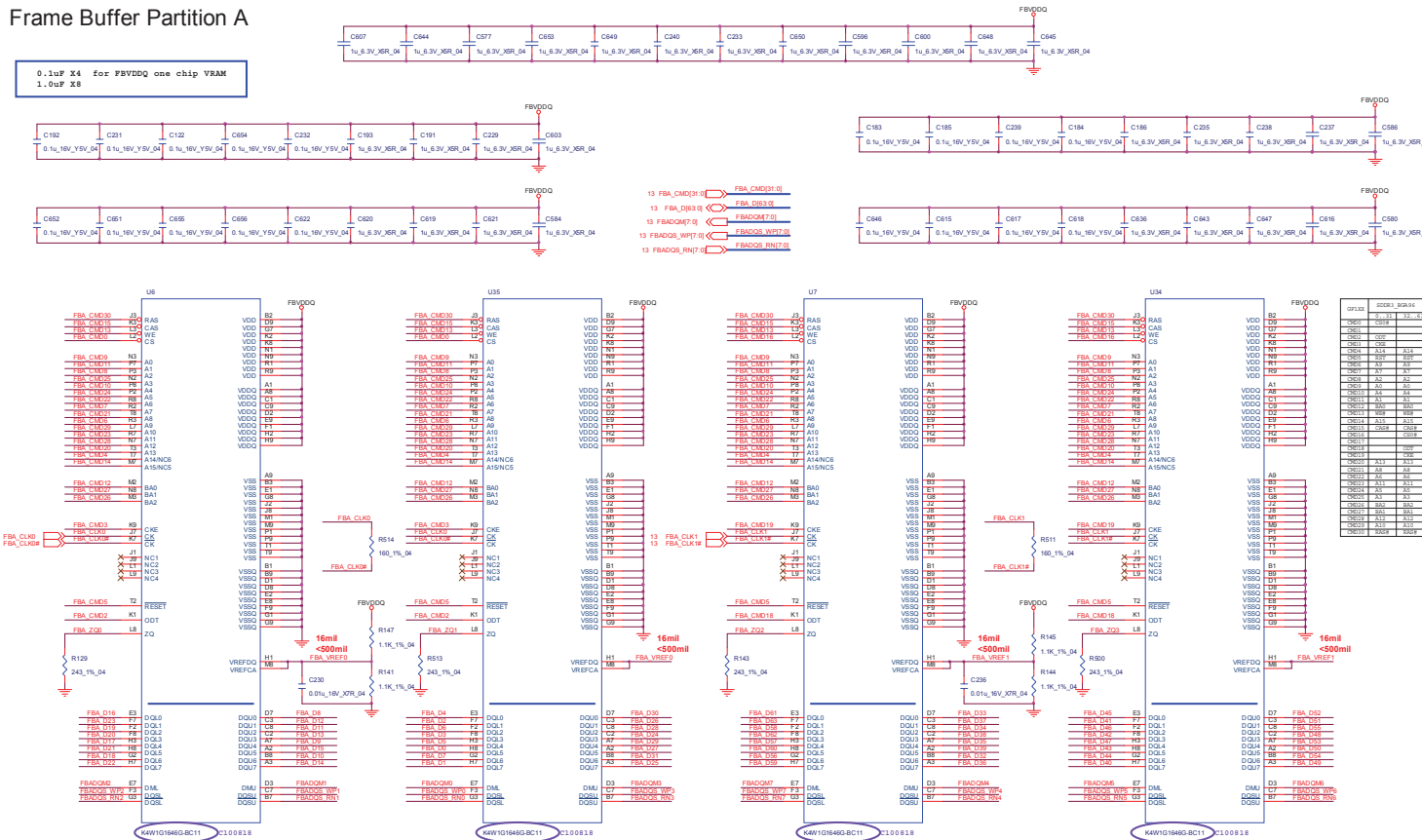
VGA Frame Buffer Interface

Frame Buffer Interface



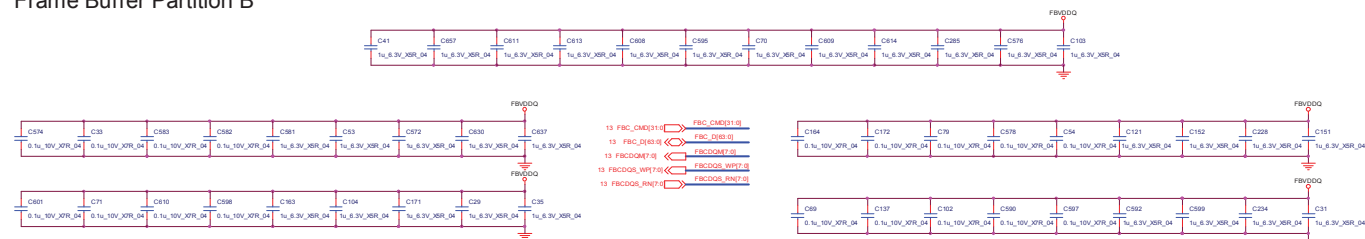
VGA Frame Buffer A

Frame Buffer Partition A

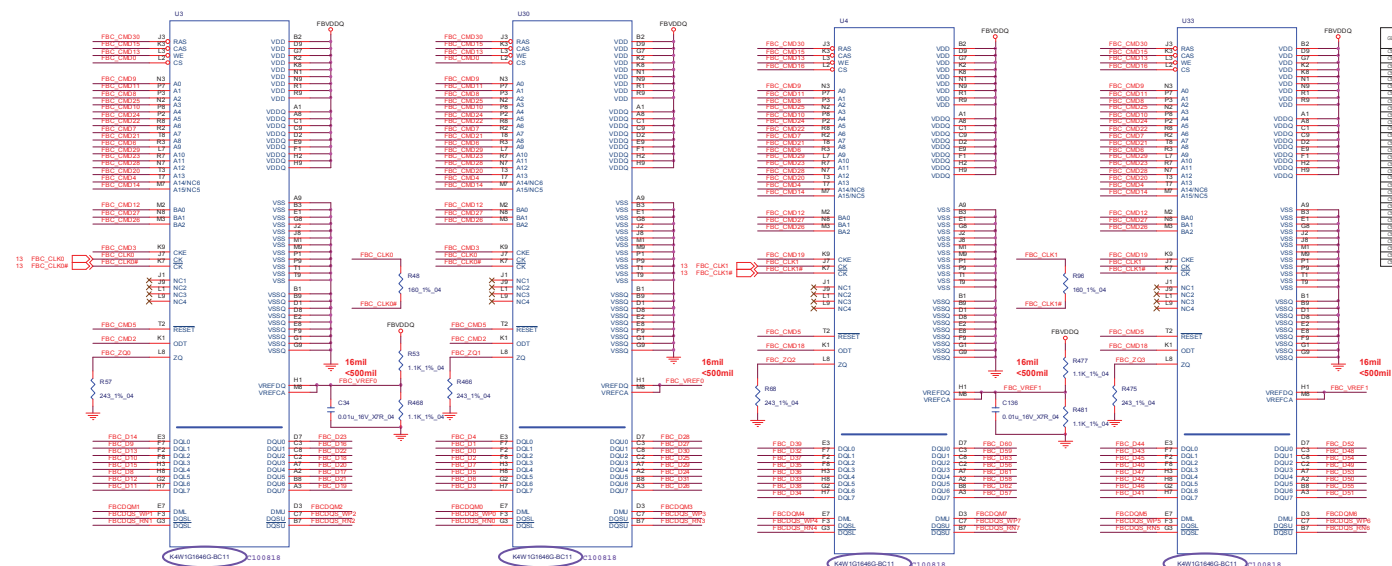
Sheet 14 of 50
VGA Frame Buffer A

VGA Frame Buffer C

Frame Buffer Partition B

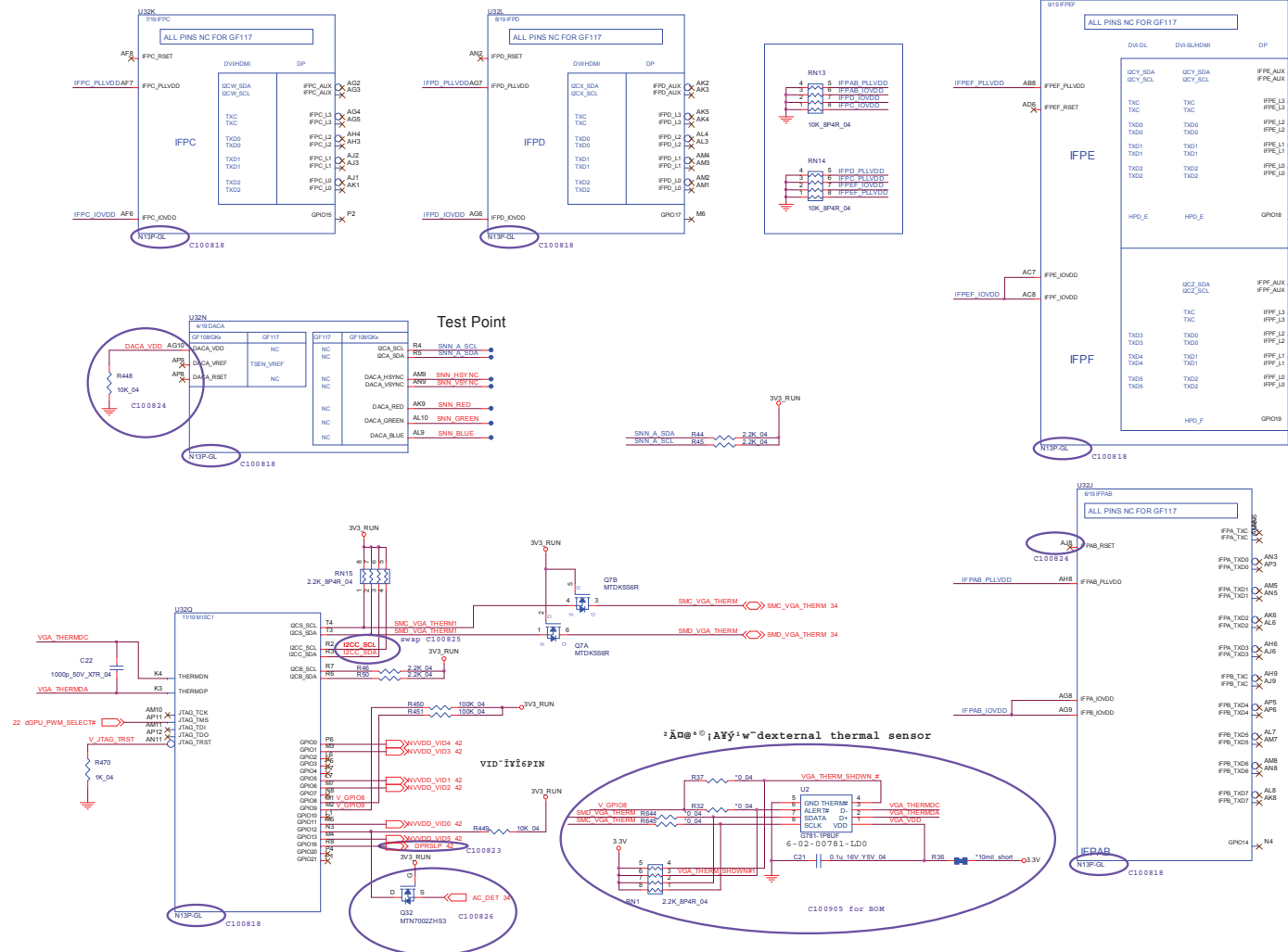


Sheet 15 of 50
VGA Frame Buffer
C



Schematic Diagrams

VGA I/O



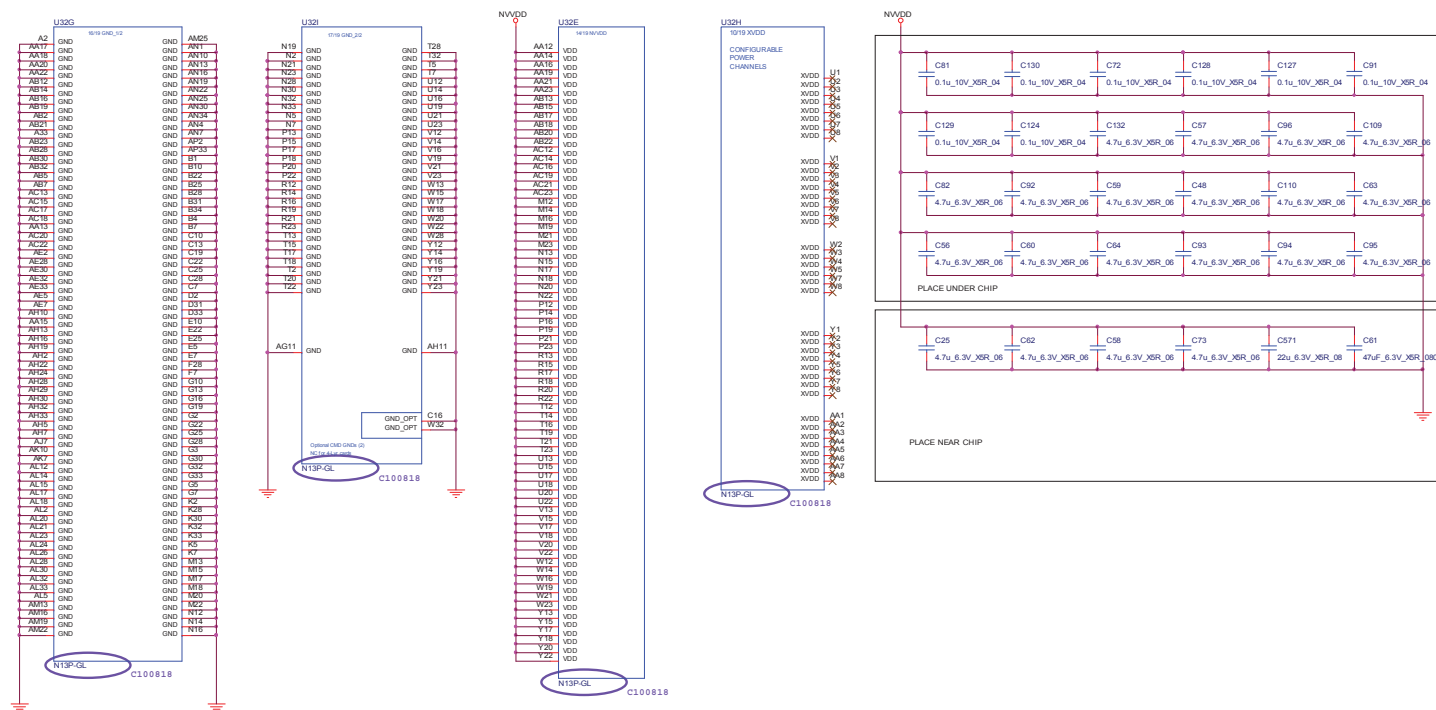
Sheet 16 of 50
VGA I/O

B.Schematic Diagrams

Schematic Diagrams

VGA NVVDD Cecoupling

Sheet 17 of 50
VGA NVVDD
Cecoupling



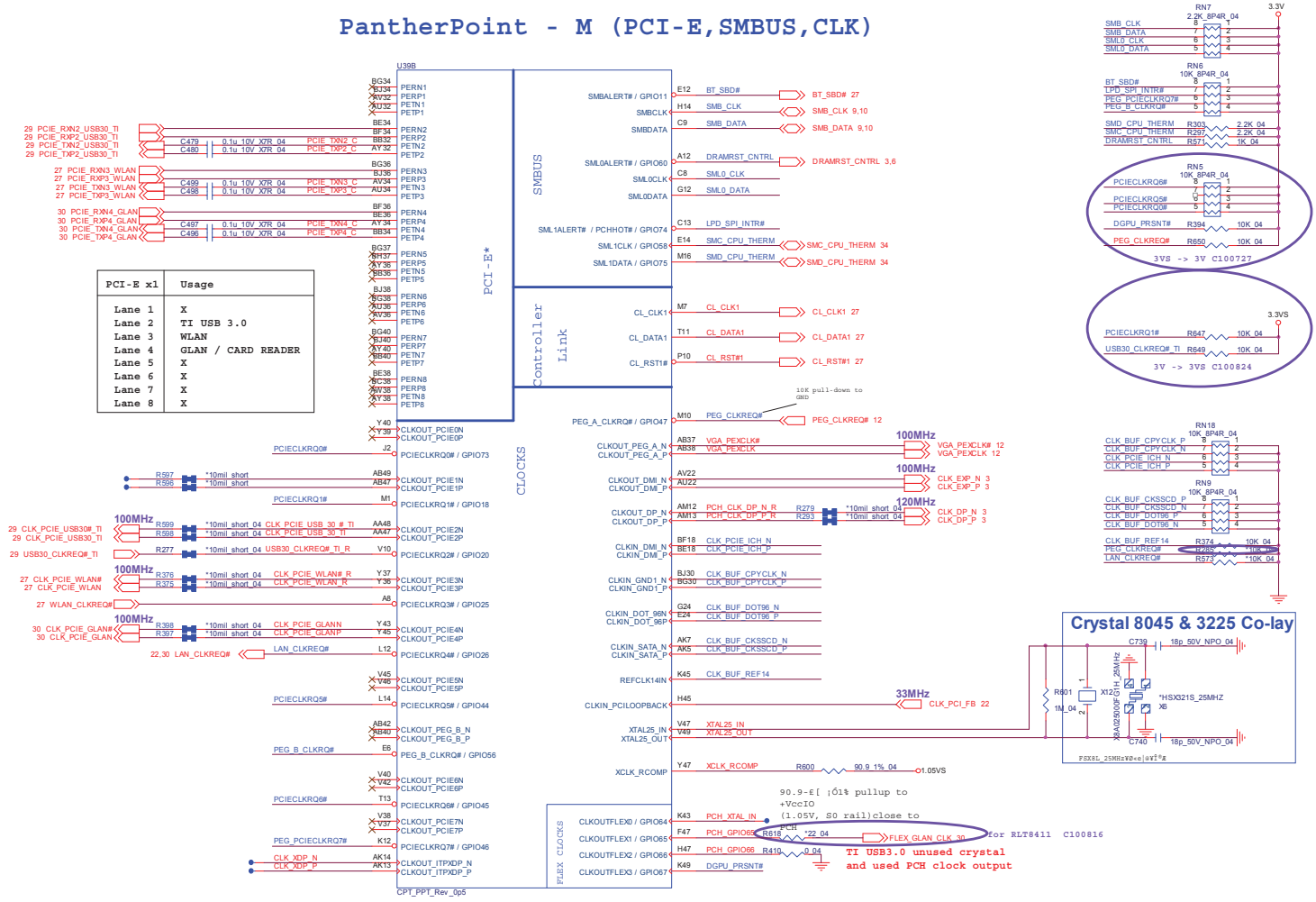
Schematic Diagrams



Schematic Diagrams

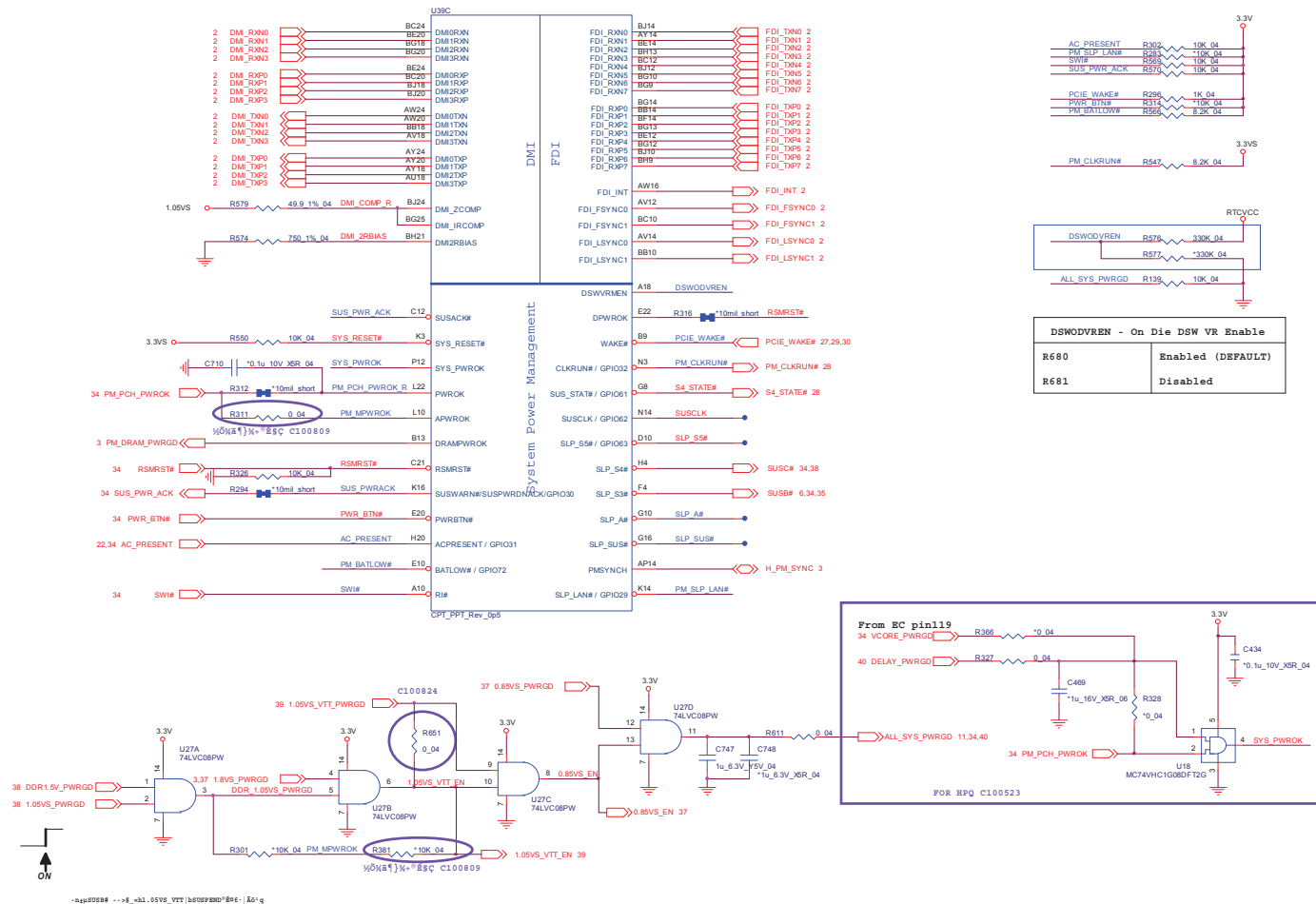
PCH 2/9- PCIE, SMBUS, CLK

Sheet 19 of 50
PCH 2/9- PCIE,
SMBUS, CLK



PCH 3/9- DMI, FDI, PWRGD

PantherPoint -M (DMI,FDI,GPIO)



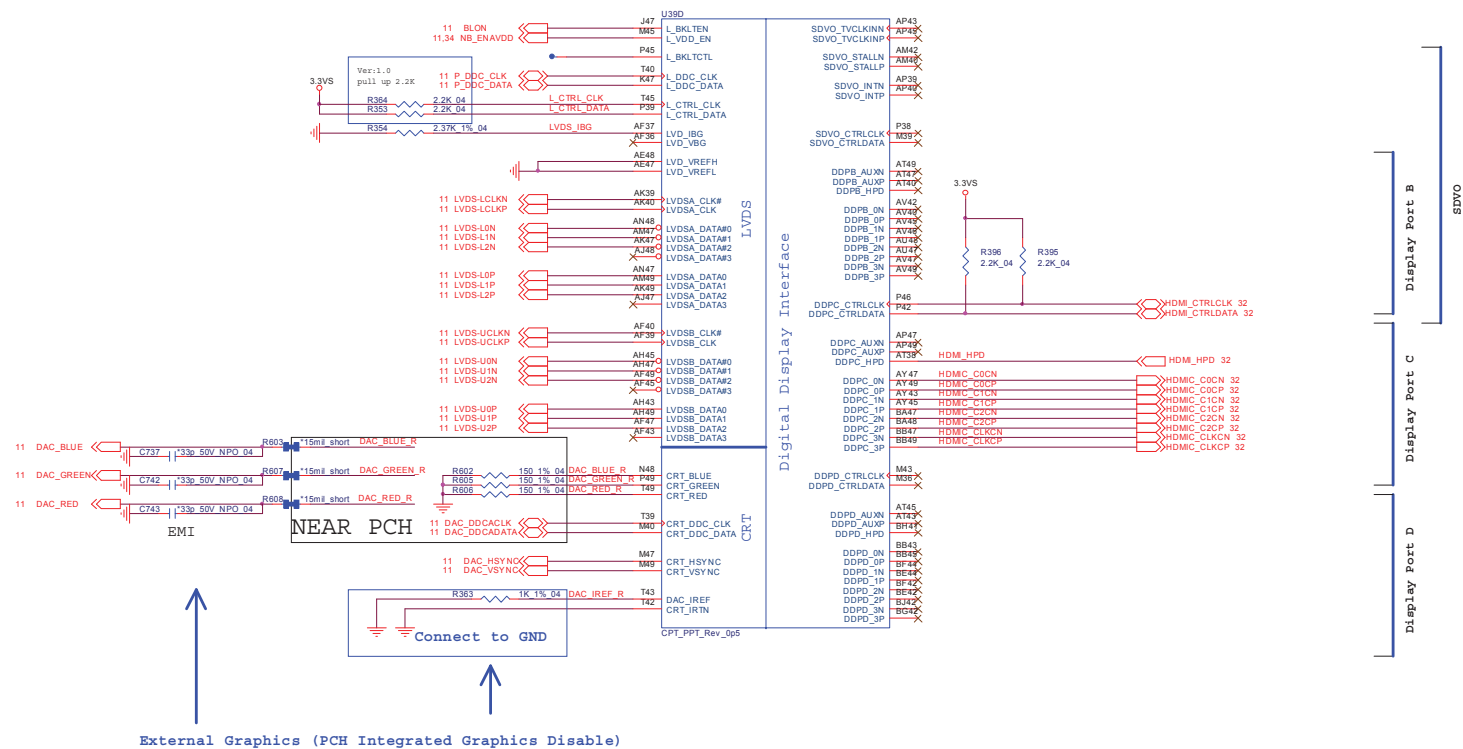
Sheet 20 of 50
PCH 3/9- DMI, FDI,
PWRGD

Schematic Diagrams

PCH 4/9- LVDS, DDI, CRT

Sheet 21 of 50
PCH 4/9- LVDS,
DDI, CRT

PantherPoint -M (LVDS,DDI)



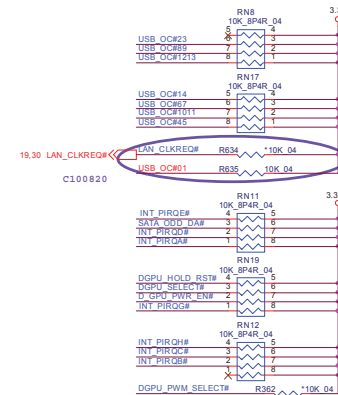
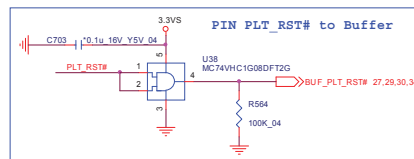
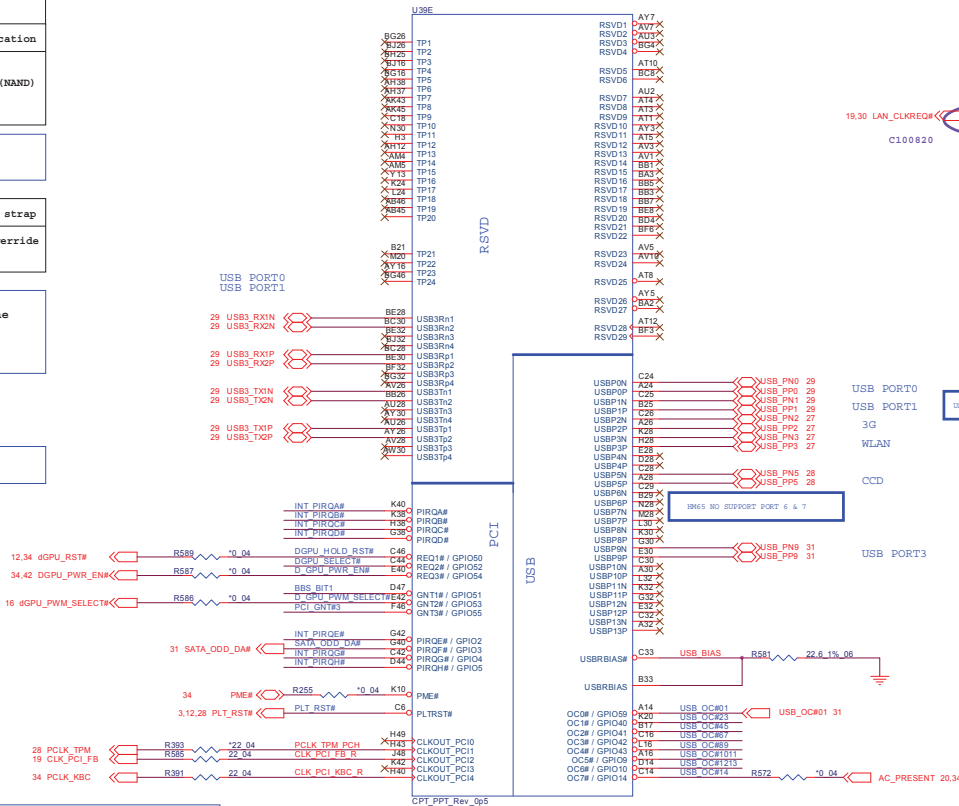
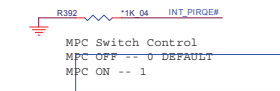
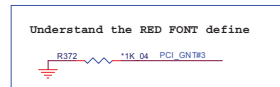
PCH 4/9- PCI, USB, RSVD

PantherPoint -M (PCI,USB,NVRAM)

| Boot BIOS Strap | | |
|-----------------|----------|--------------------|
| BBS_BIT1 | BBS_BIT0 | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |



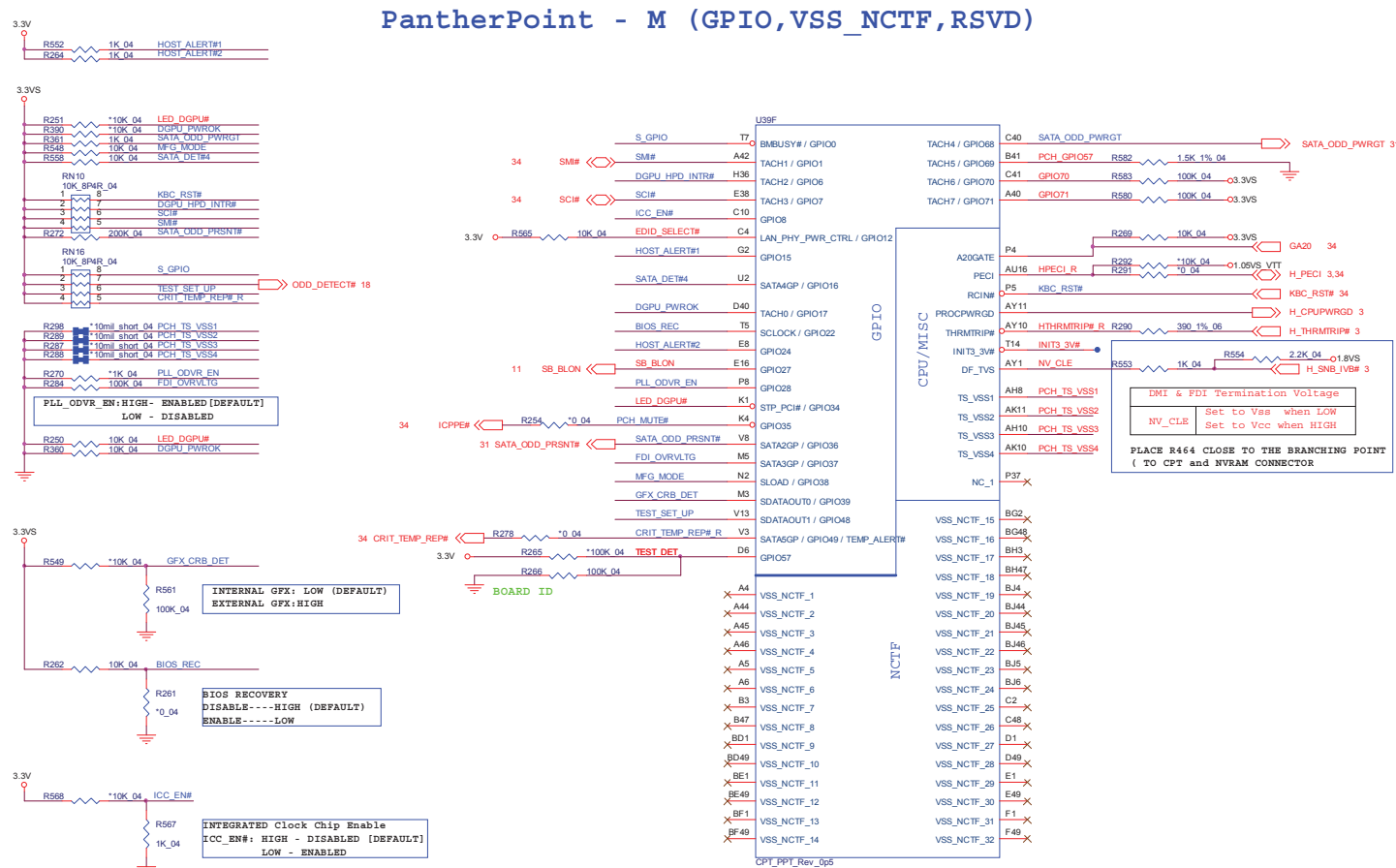
| Flash Descriptor security override strap | |
|--|---|
| PCI_GNT#3 | LOW = PCI_GNT#3 swap override HIGH = Default |



Sheet 22 of 50
PCH 4/9- PCI, USB,
RSVD

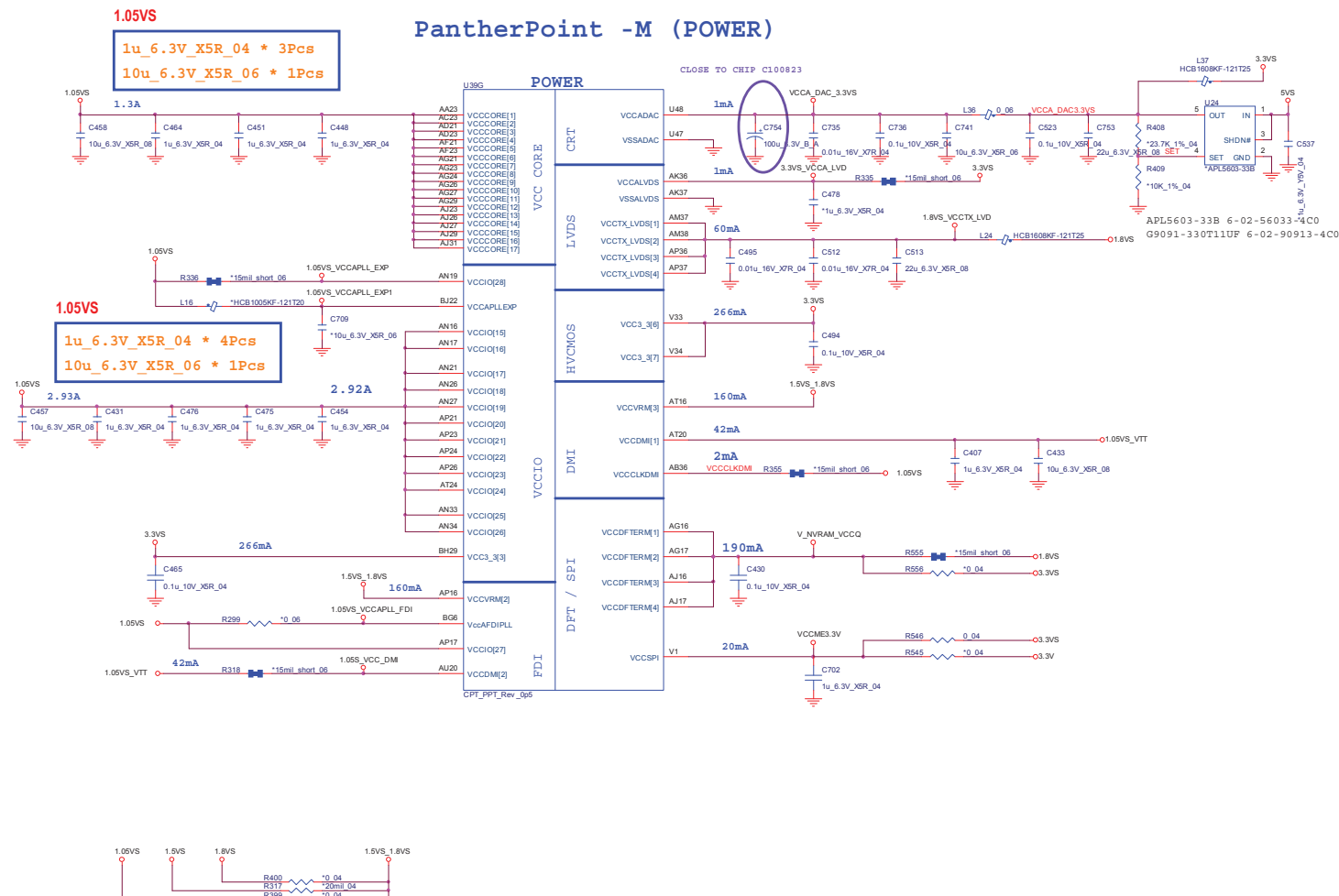
PCH 6/9- GPIO, CPU

Sheet 23 of 50
PCH 6/9- GPIO,
CPU



PCH 7/9- PWR B - 25

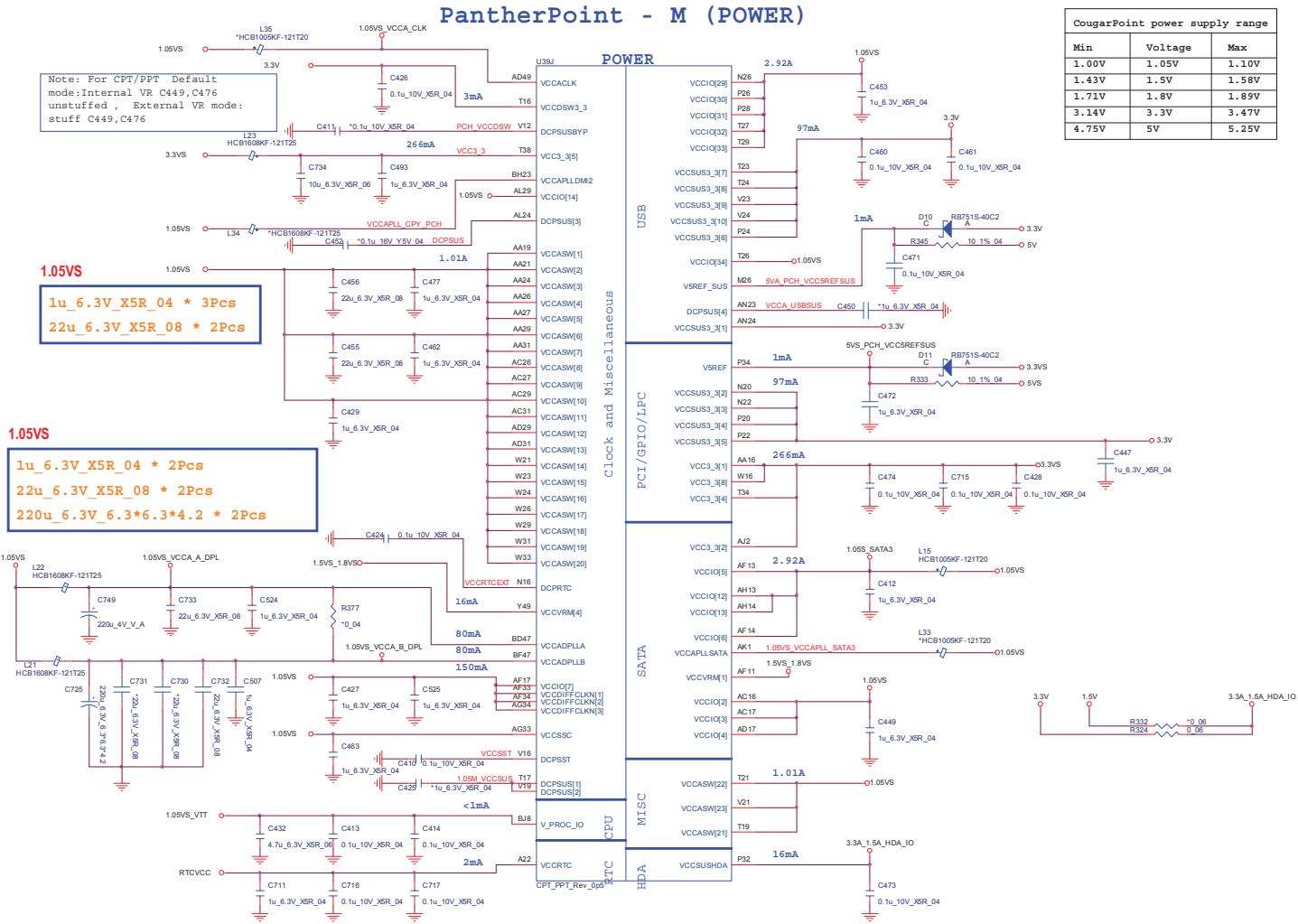
B.Schematic Diagrams



Schematic Diagrams

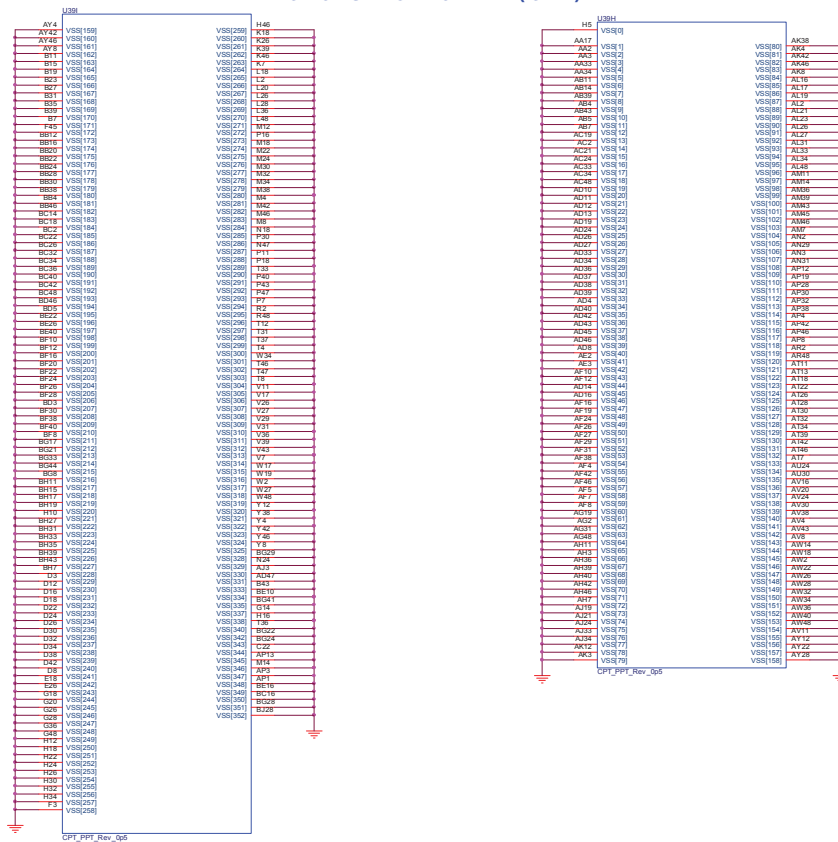
PCH 8/9 POWER

Sheet 25 of 50
PCH 8/9 POWER



PCH 9/9- GND

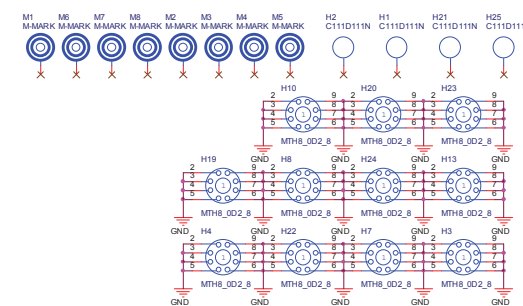
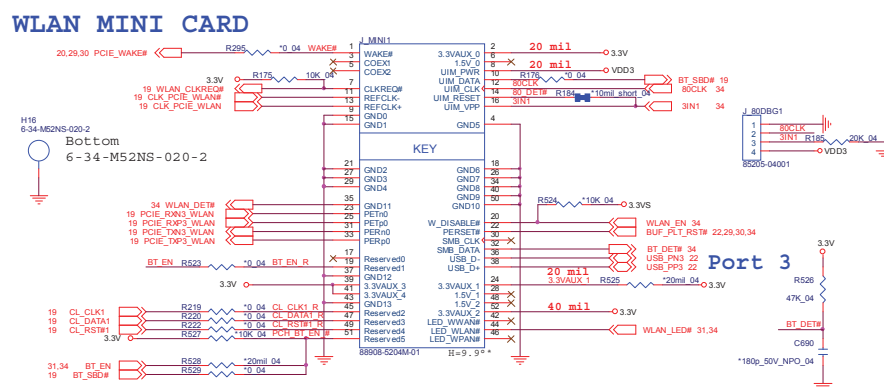
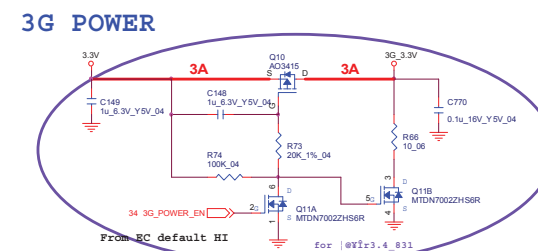
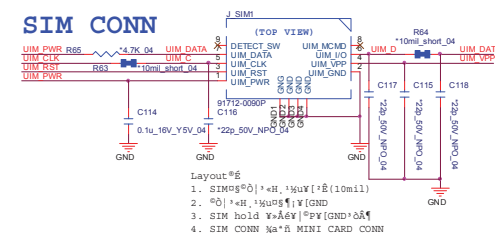
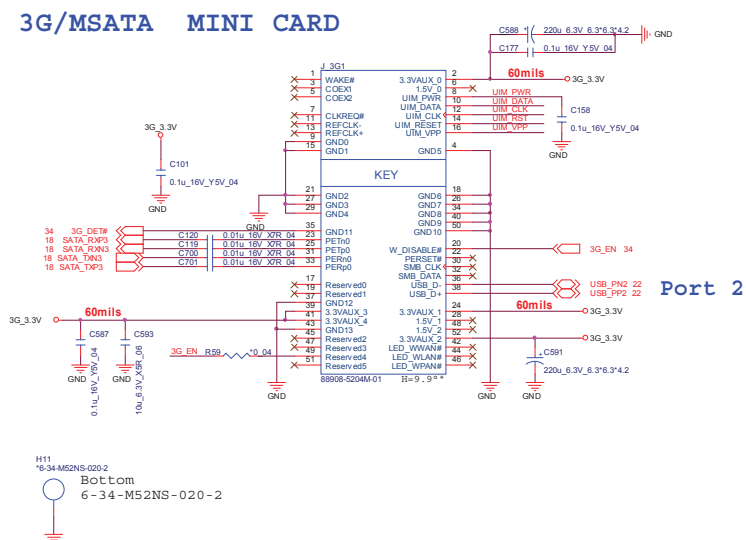
PantherPoint -M (GND)



| Voltage Rail | Voltage | 50 Iccmax Current (A) |
|--------------|---------|-----------------------|
| V_CPU_IO | 1.05 | 1 (mA) |
| VSRFP_Sus | 5 | 1 (mA) |
| Vcc3_3 | 3.3 | 0.266 |
| VccADAC3 | 1.05 | 1 (mA) |
| VccADPLLA | 1.05 | 0.08 |
| VccADPLLB | 1.05 | 0.08 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.1 | 0.042 |
| VccIO | 1.05 | 2.925 |
| VccASW | 1.05 | 1.01 |
| VccSPI | 3.3 | 0.020 |
| VccDWD3_3 | 3.3 | 2 (mA) |
| VccDPTERM | 1.8 | 0.19 |
| VccSus3_3 | 3.3 | 0.097 |
| VccSusHDA | 3.3 | 1 (mA) |
| VccVPM | 1.5 | 0.16 |
| VccCLKDMI | 1.05 | 0.02 |
| VccSBC | 1.05 | 0.095 |
| VccDIFFCLKM | 1.05 | 0.055 |
| VccALVDS | 3.3 | 1 (mA) |
| VccTX_LVDS | 1.8 | 0.06 |

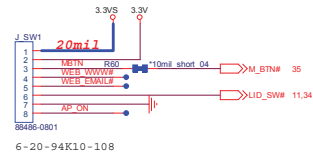
Sheet 26 of 50
PCH 9/9- GND

WLAN, 3G, MINI PCIE



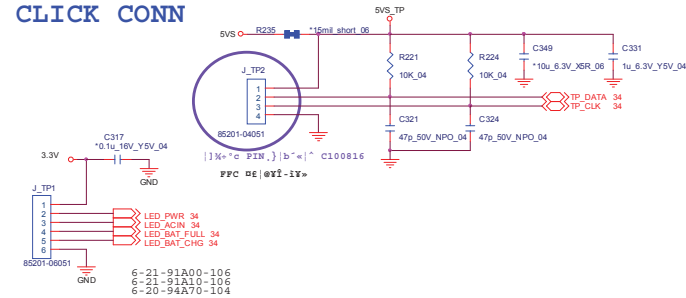
CCD, TPM, MULTI CON

FOR POWER SW BOARD

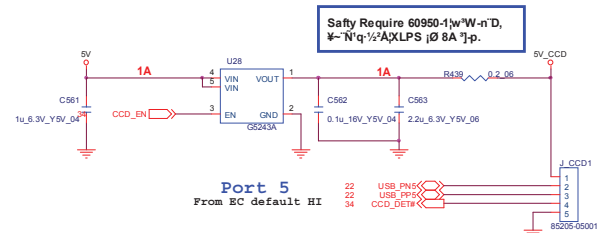


FOR OPTIMUS FUNCTION

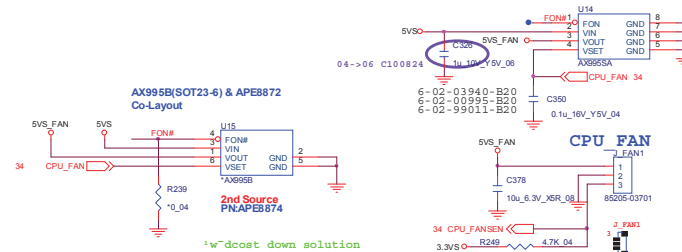
CLICK CONN



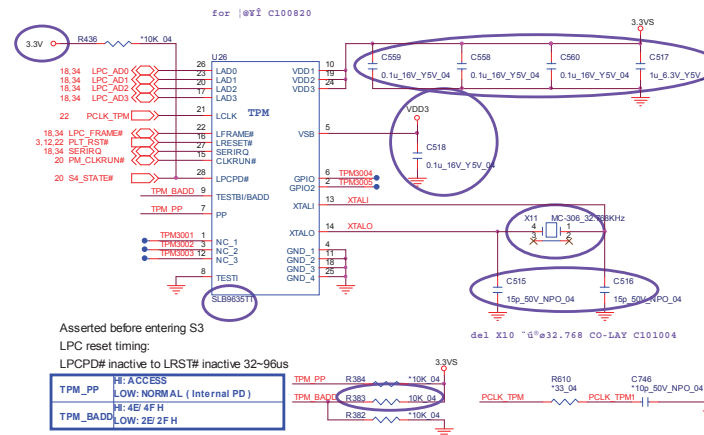
CCD



CPU FAN CONTROL



TPM 1.2

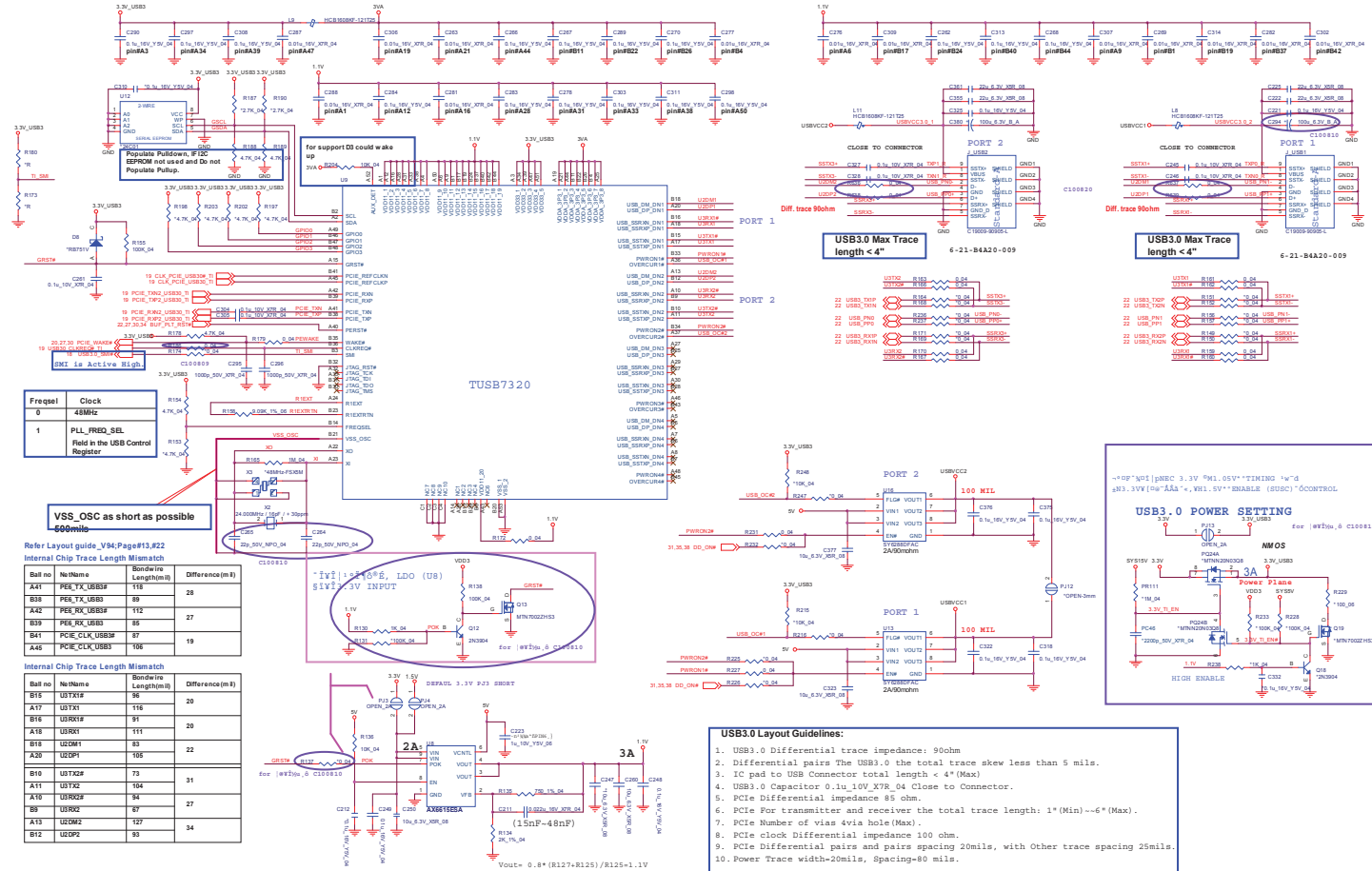


Sheet 28 of 50
CCD, TPM, MULTI
CON

Schematic Diagrams

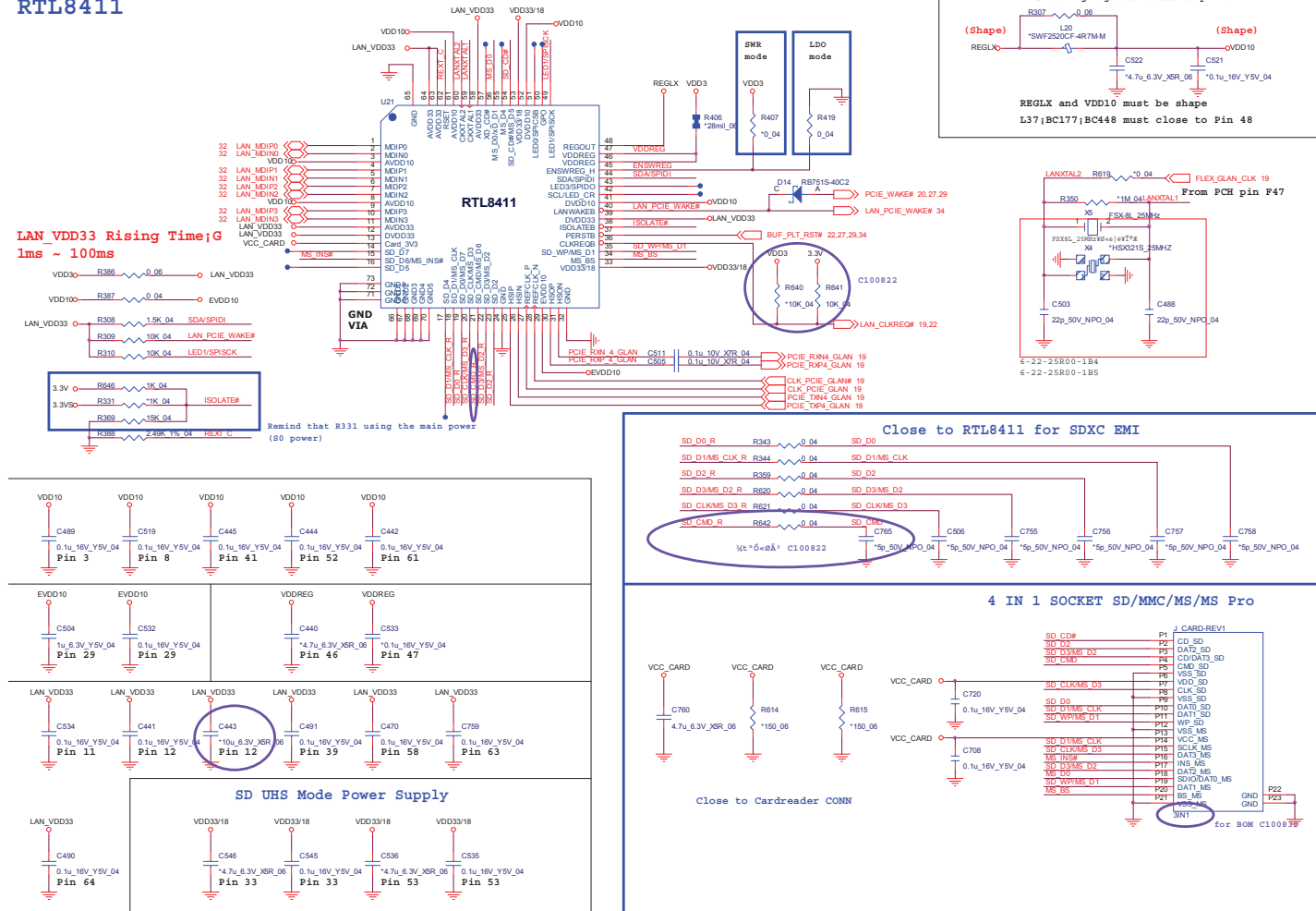
USB3.0

Sheet 29 of 50
USB3.0



Card Reader (RTL8411)

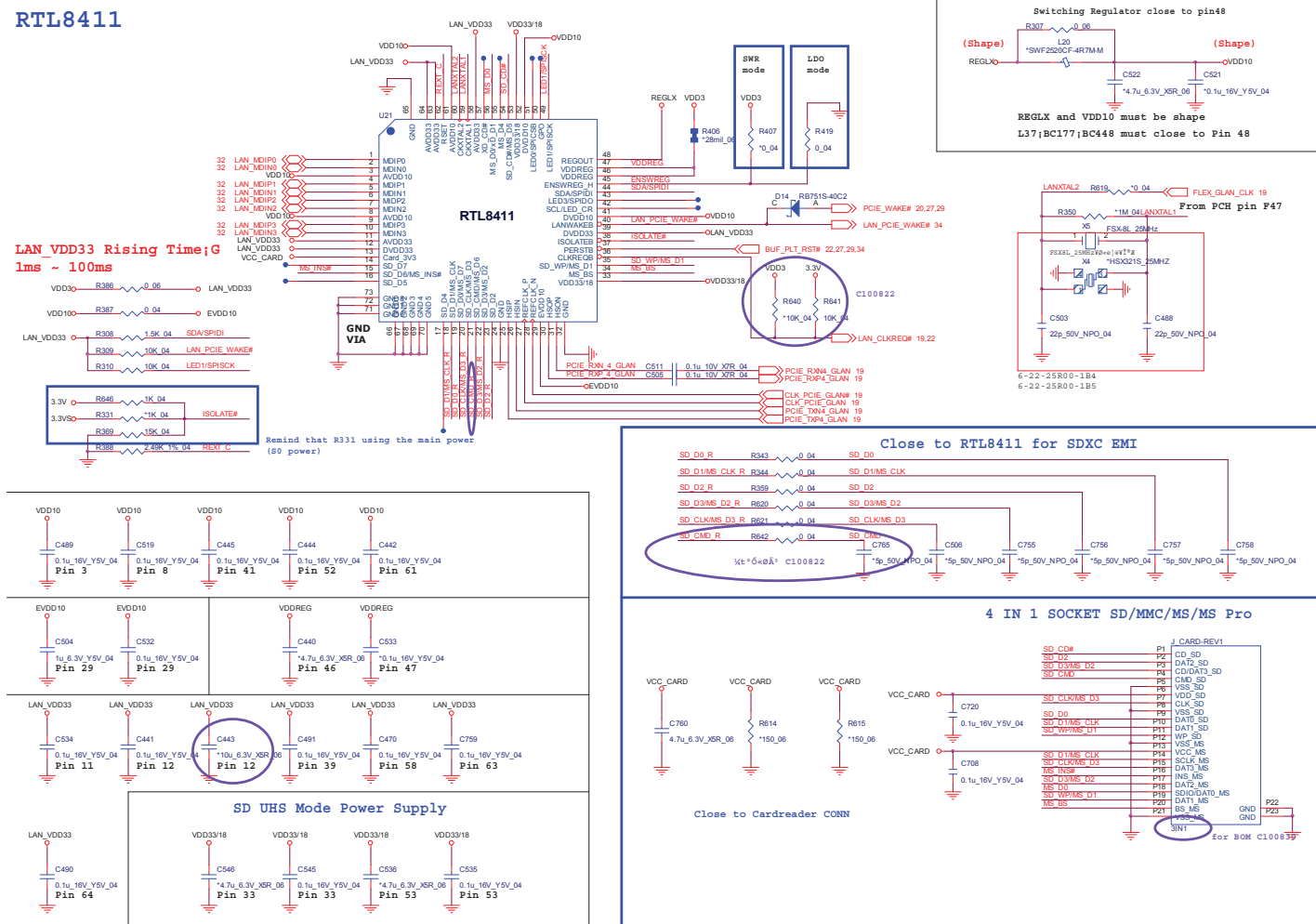
RTL8411



Sheet 30 of 50
Card Reader
(RTL8411)

B.Schematic Diagrams

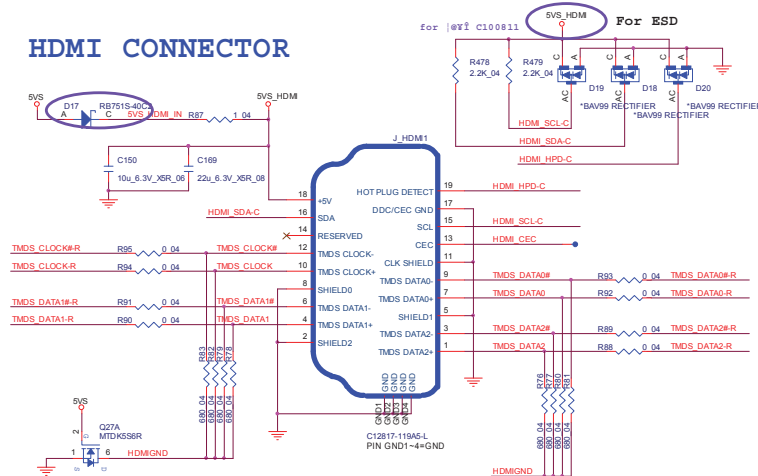
Sheet 31 of 50
SATA ODD, LED,
USB CHARGE



LAN PORT GIGA LAN (JMC251C)

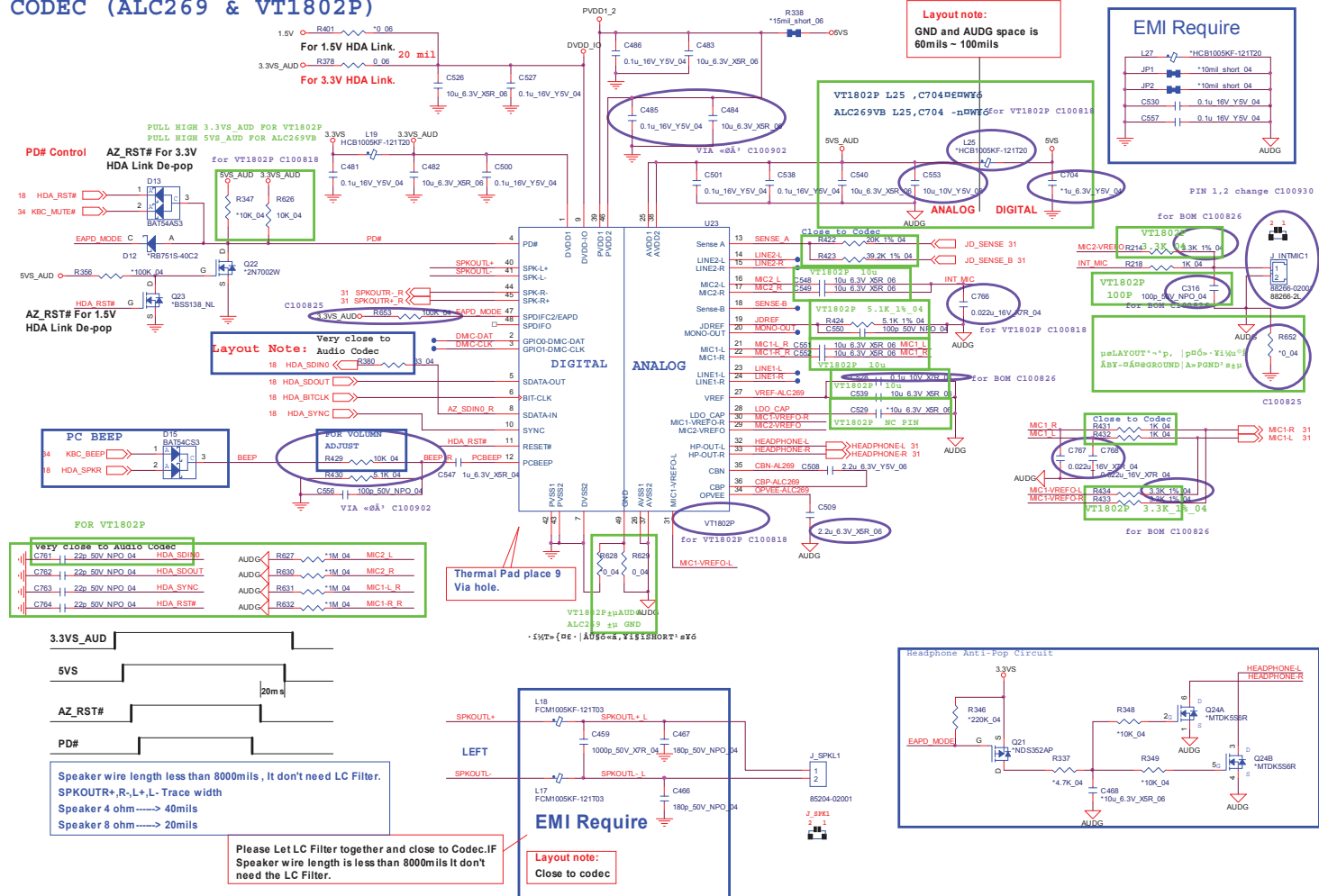


HDMI CONNECTOR



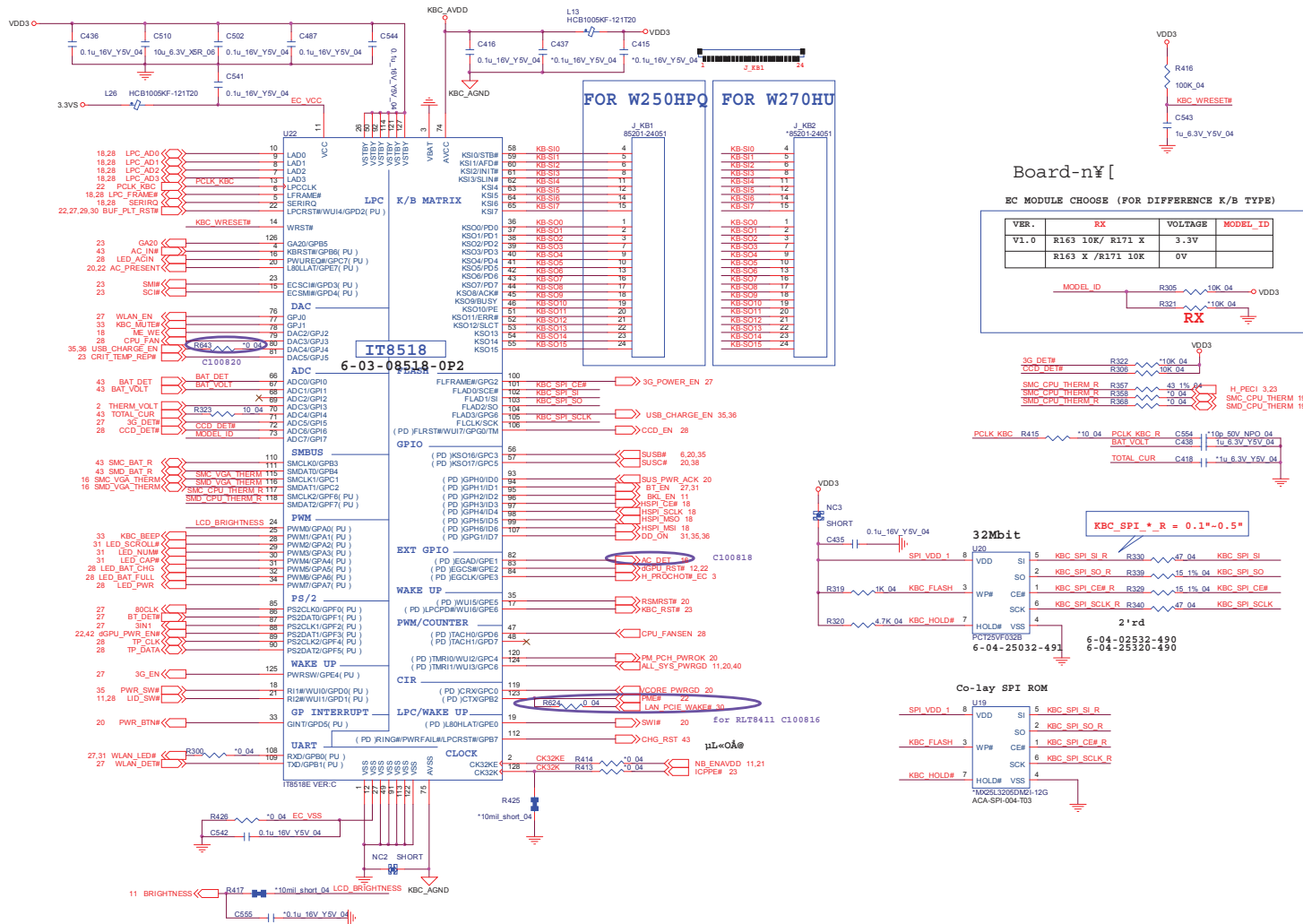
AUDIO CODEC VT1802P

CODEC (ALC269 & VT1802P)



Sheet 33 of 50
AUDIO CODEC
VT1802P

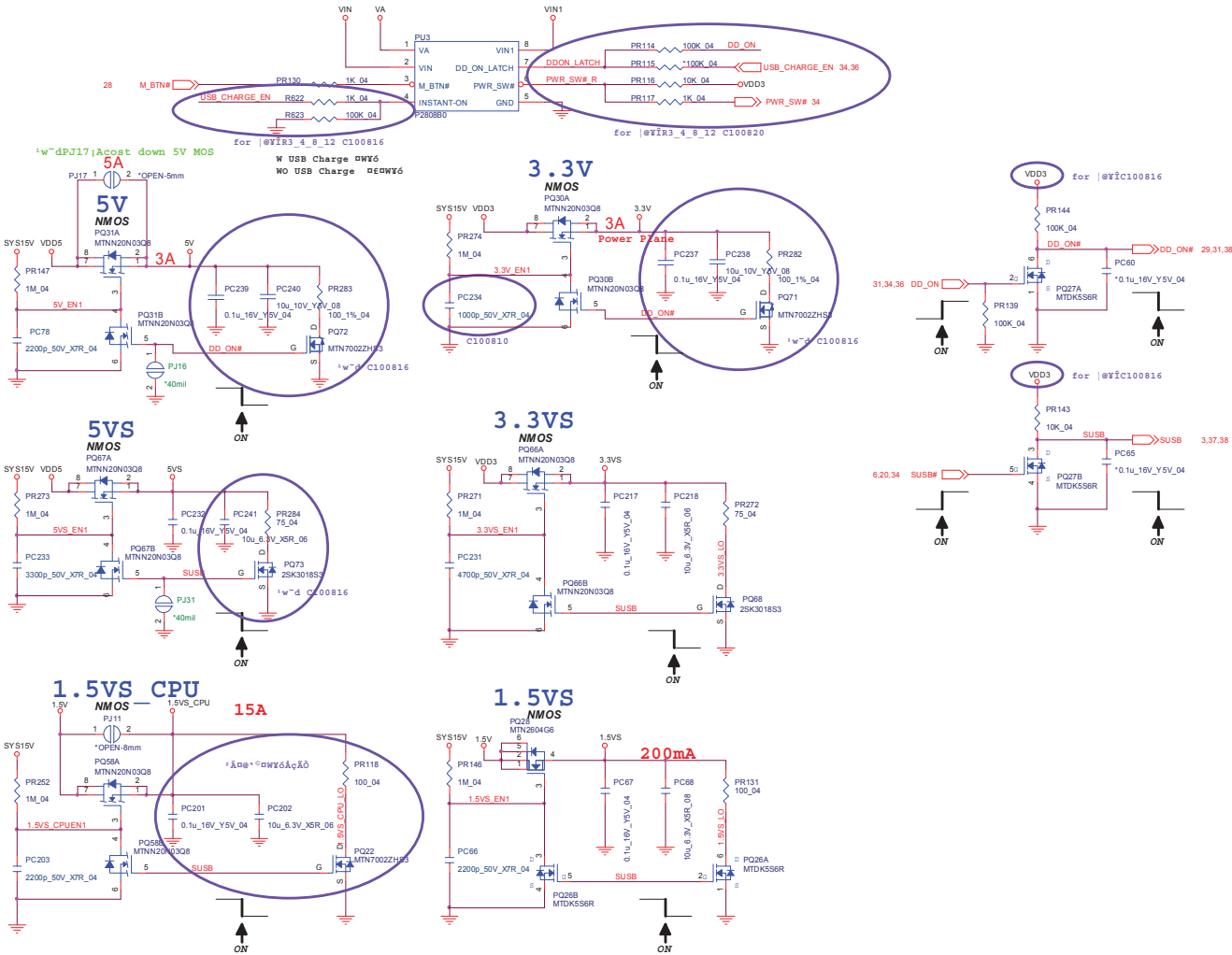
KBC-ITE IT8518E



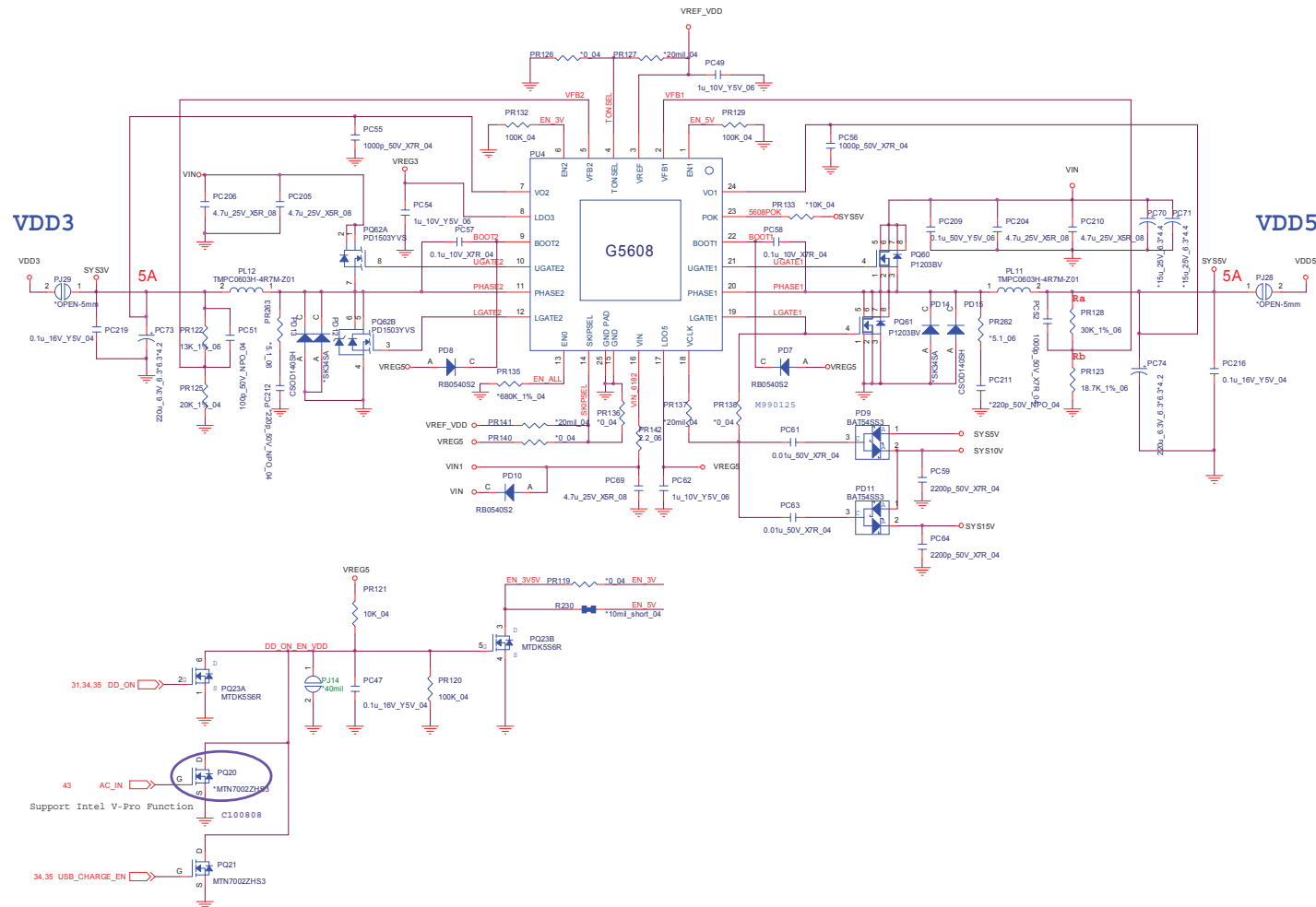
Schematic Diagrams

5VS, 3VS, 1.5VS CPU

Sheet 35 of 50
5VS, 3VS, 1.5VS
CPU

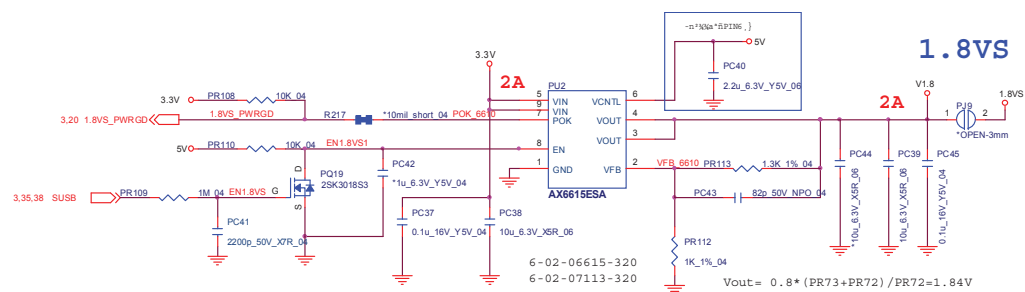


VDD3, VDD5

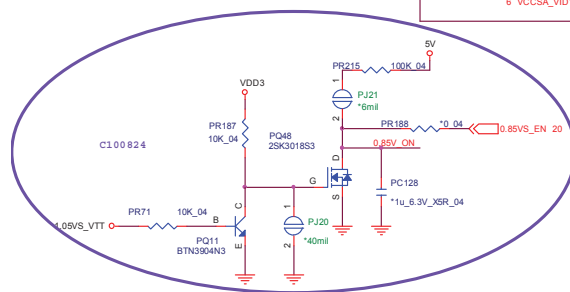
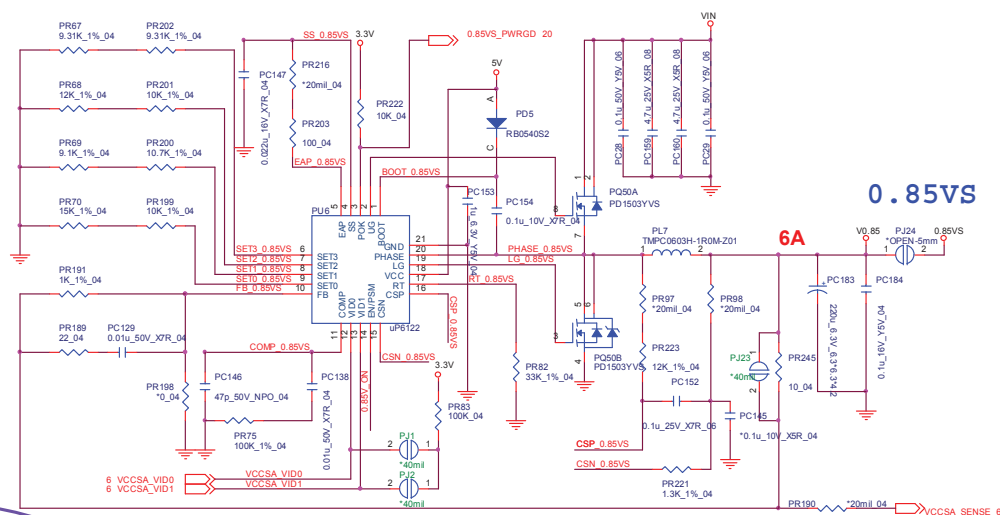


Sheet 36 of 50
VDD3, VDD5

Power 0.85VS, 1.8VS

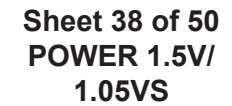


Sheet 37 of 50
Power 0.85VS,
1.8VS



| | 0.9V | 0.8V | 0.725V | 0.675V |
|------------|------|------|--------|--------|
| VCCSA_VID0 | 0 | 0 | 1 | 1 |
| VCCSA_VID1 | 0 | 1 | 0 | 1 |

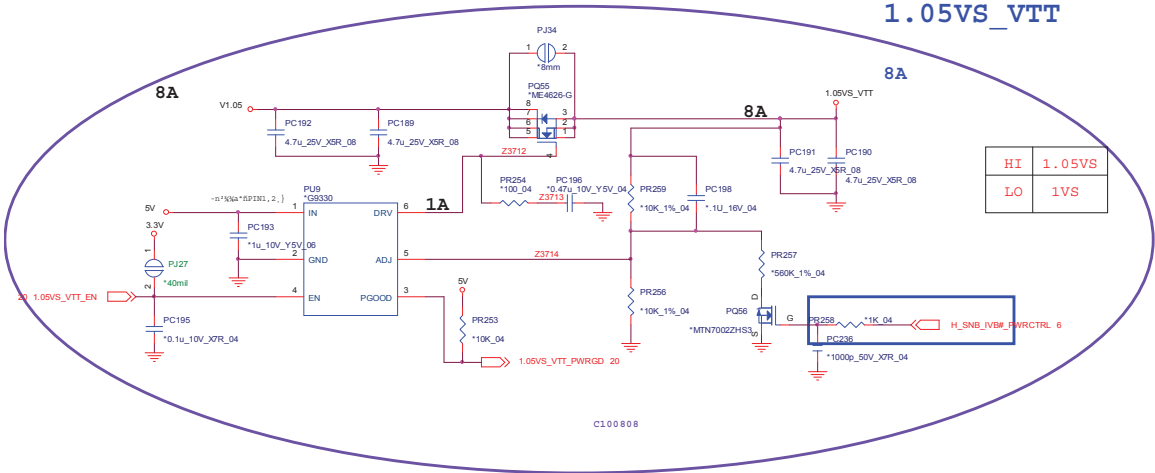
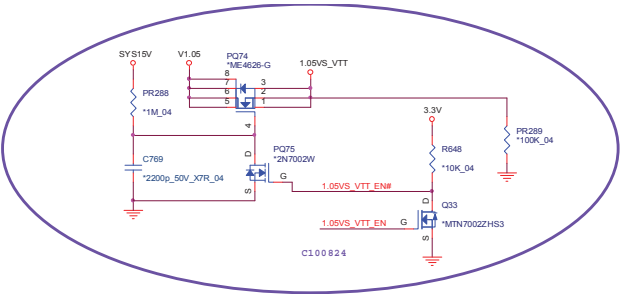
VTT_MEM



Schematic Diagrams

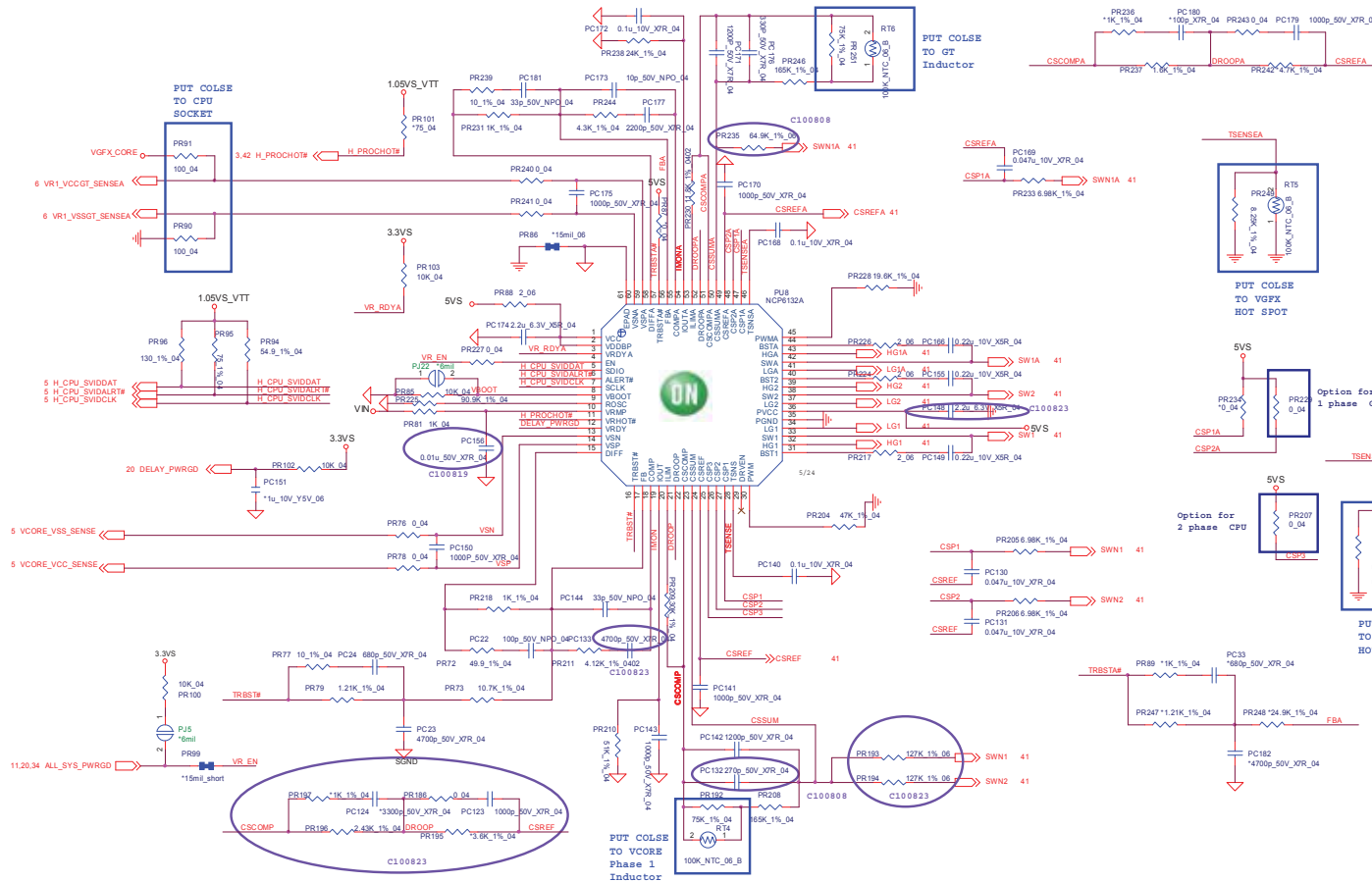
POWER 1.05V/1.05VS VTT

Sheet 39 of 50
POWER 1.05VS/
1.05VS VTT



| | |
|----|--------|
| HI | 1.05VS |
| LO | 1VS |

POWER VCORE1

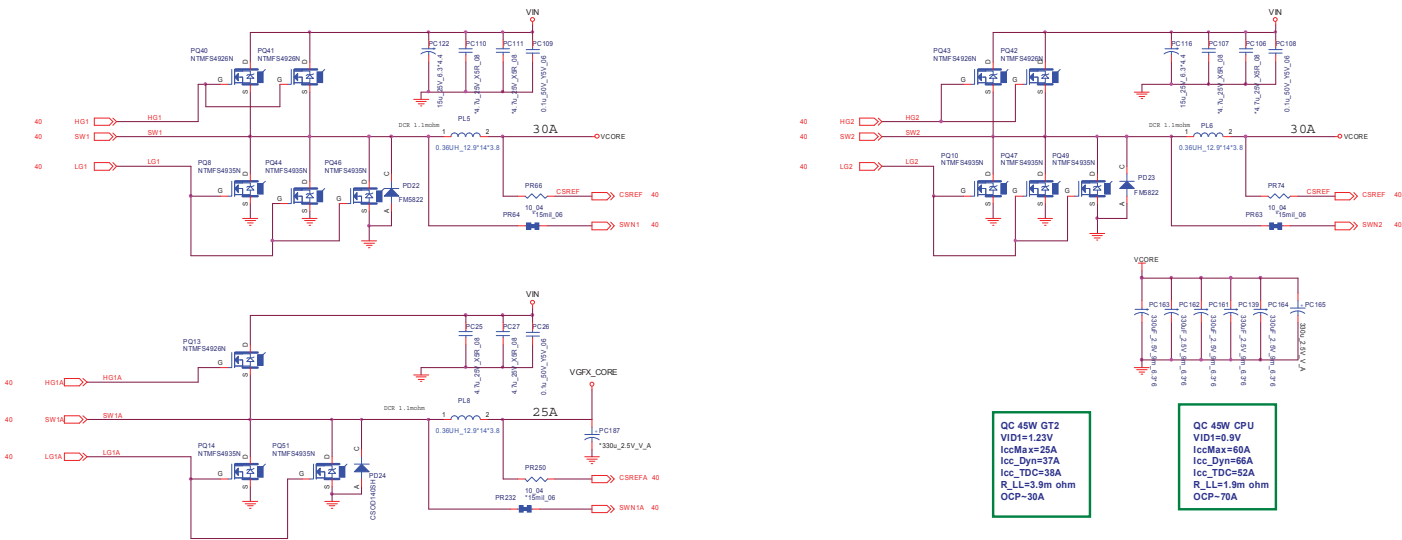


Sheet 40 of 50
POWER VCORE1

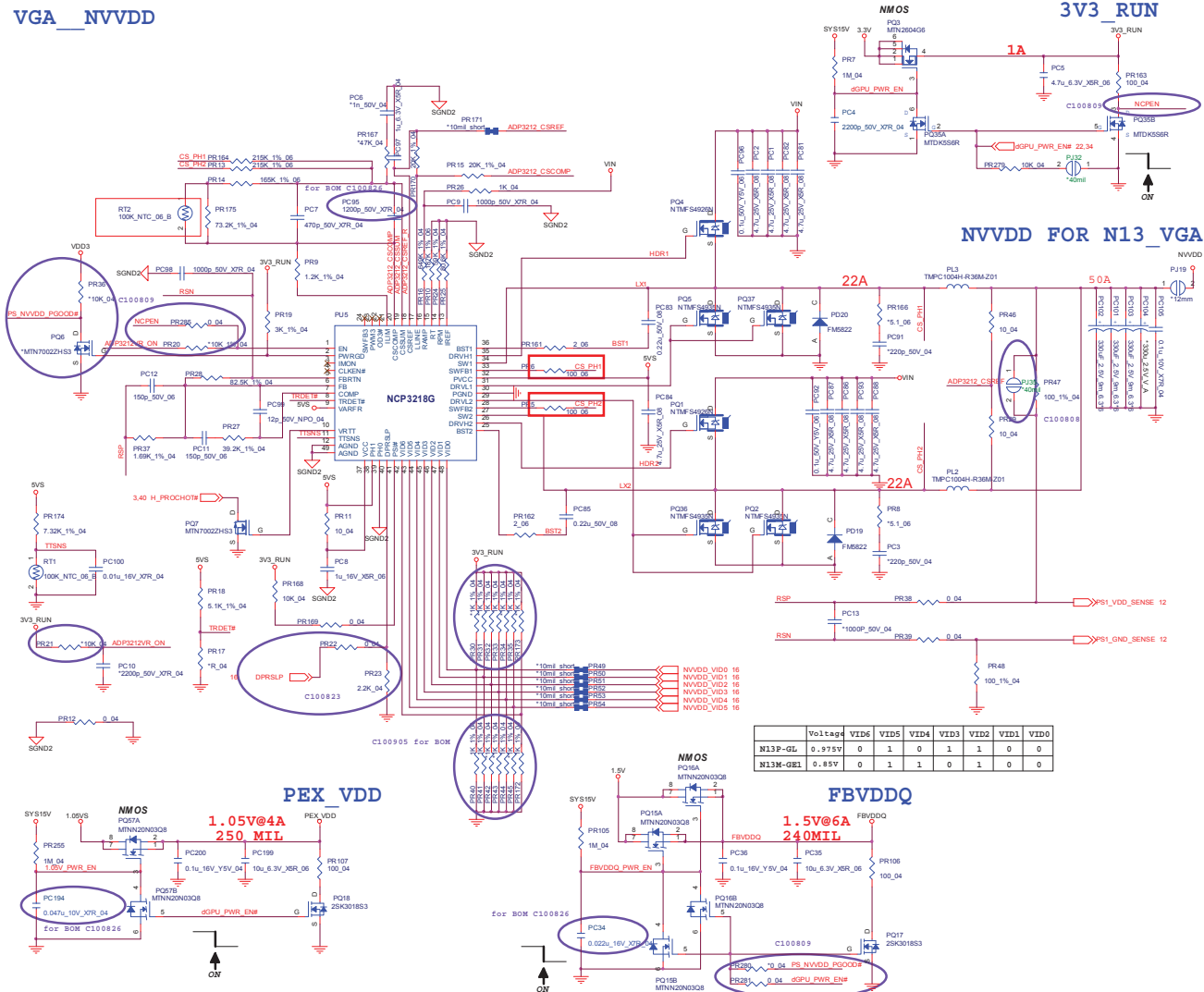
Schematic Diagrams

POWER VCORE2

Sheet 41 of 50
POWER VCORE2

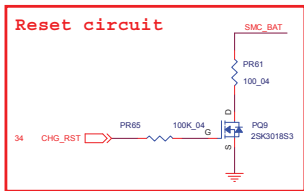


Power VGA NVVDD/PEX_VDD



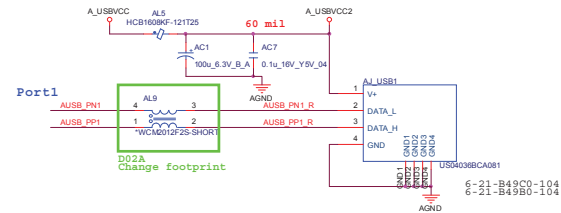
Sheet 42 of 50
Power VGA
NVVDD/PEX_VDD

Sheet 43 of 50
AC IN, CHARGER

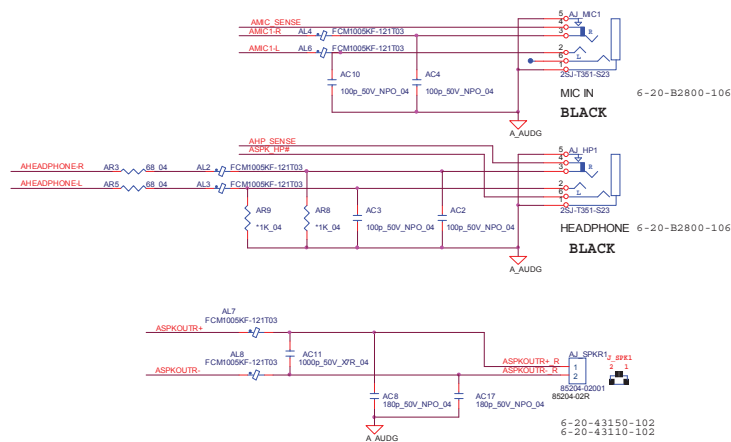
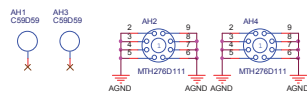
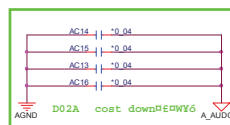
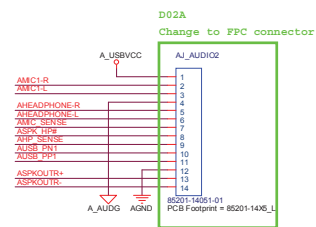


- 1) All power traces should be routed on the outer layers
GNDP, VAD, VSY5, LX, VQHG, VBATT
- 2) Use Kelvin connections for R3, R4
(separate force and measurement traces)
- 3) R23 and R24 are dummy resistors, for layout purposes only
(serves as single point connection between GNDP & GND4)
- 4) Footprint TO-236 is equivalent to SOT-23
- 5) Footprint S1P1P is a single hole axial pad
- 6) All resistors, capacitors and semiconductors are SMD
- 7) Potentiometers, and test points are axial devices

USB PORT



AUDIO JACK



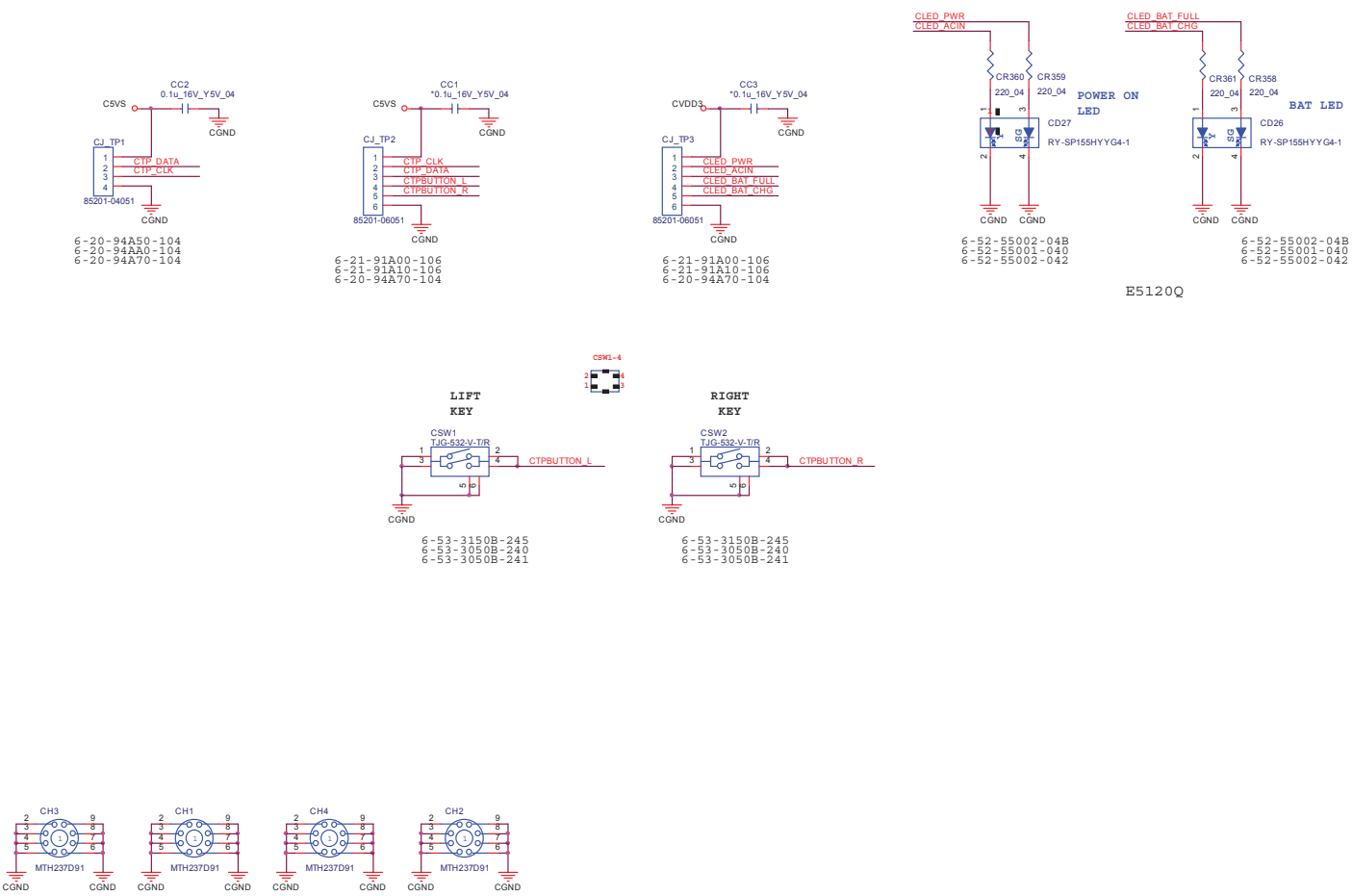
Sheet 44 of 50
AUDIO BOARD

Schematic Diagrams

CLICK BOARD

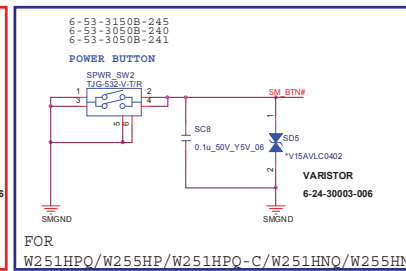
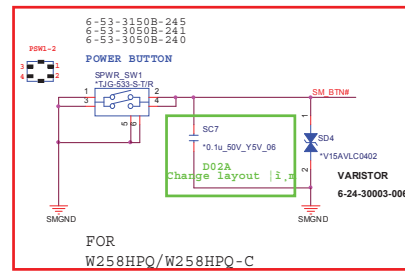
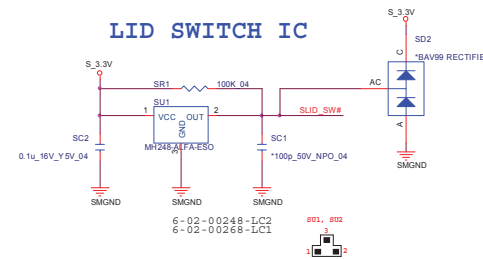
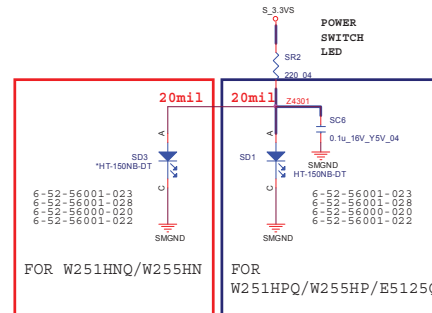
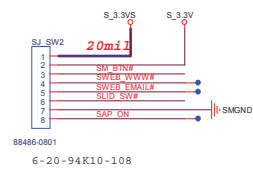
CLICK BOARD

Sheet 45 of 50
CLICK BOARD

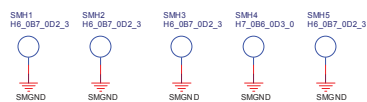


W251HPQ POWER SW BOARD

POWER SW & LED



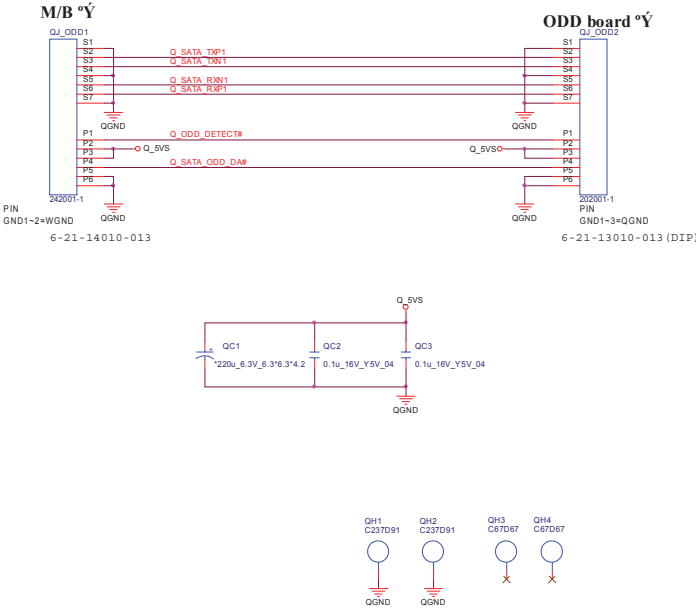
Sheet 46 of 50
W251HPQ POWER
SW BOARD



W270HU BRIDGE ODD BOARD

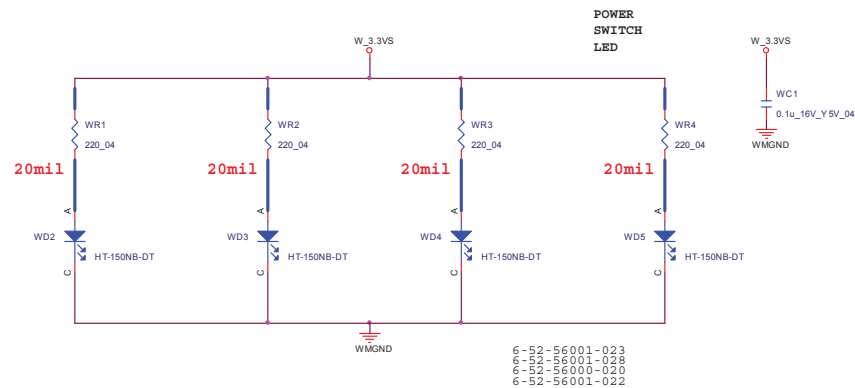
ODD BOARD FOR W270HU

Sheet 47 of 50
W270HU BRIDGE
ODD BOARD

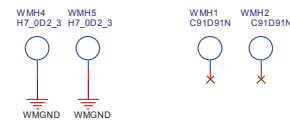
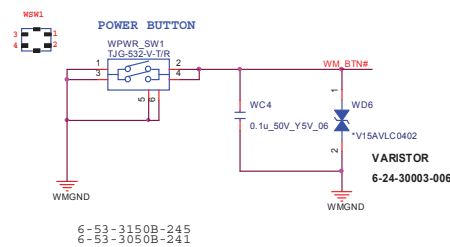
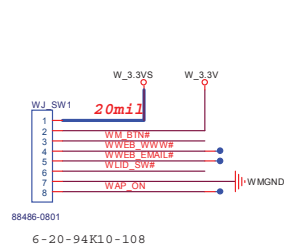
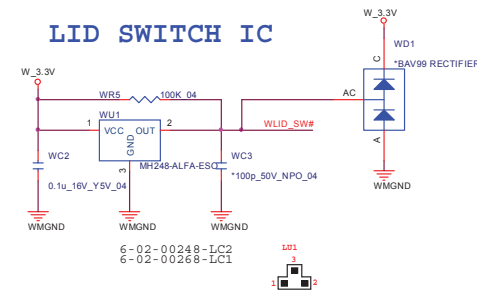


W270HU POWER SW BOARD

POWER SW & LED



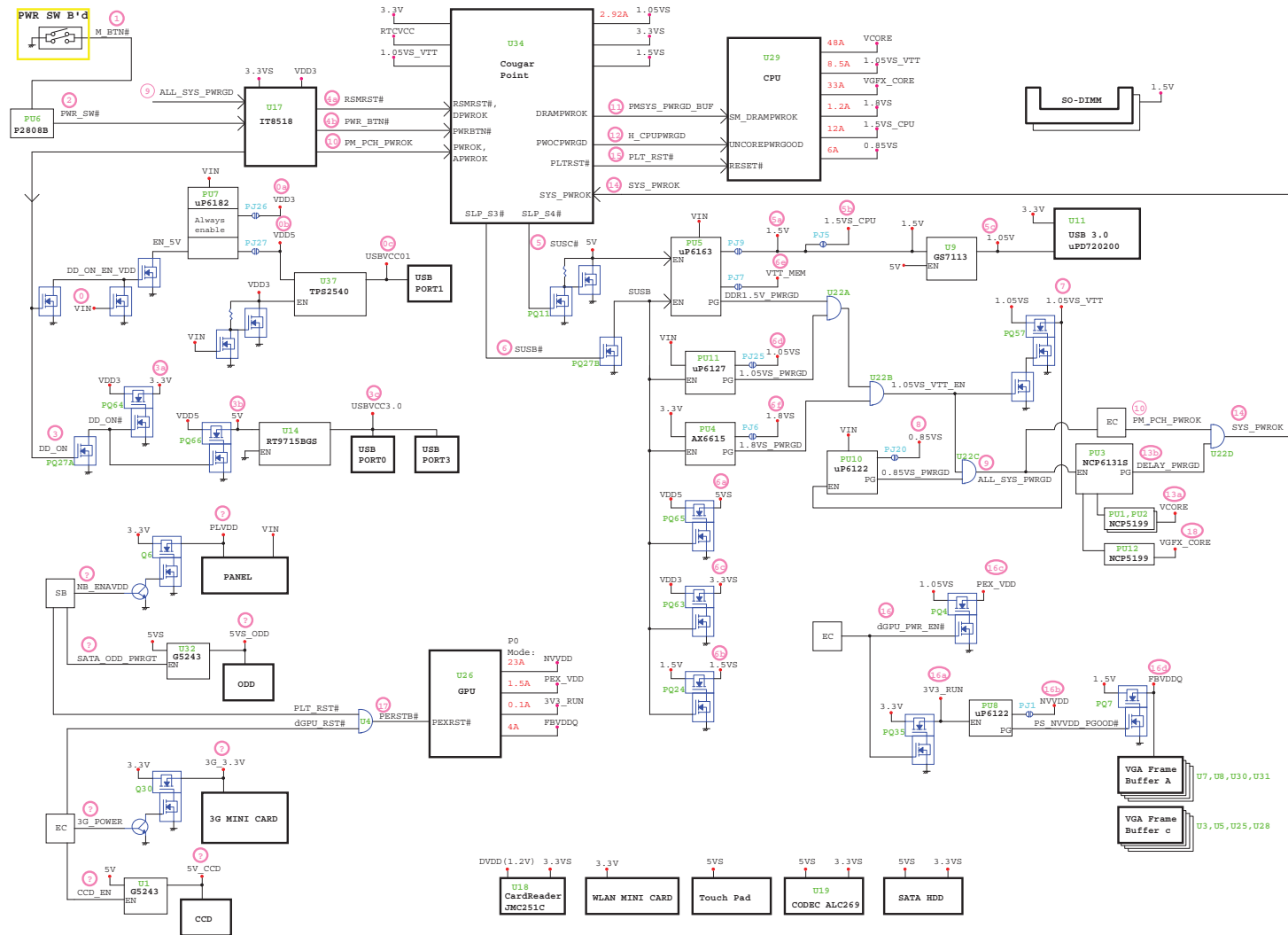
LID SWITCH IC



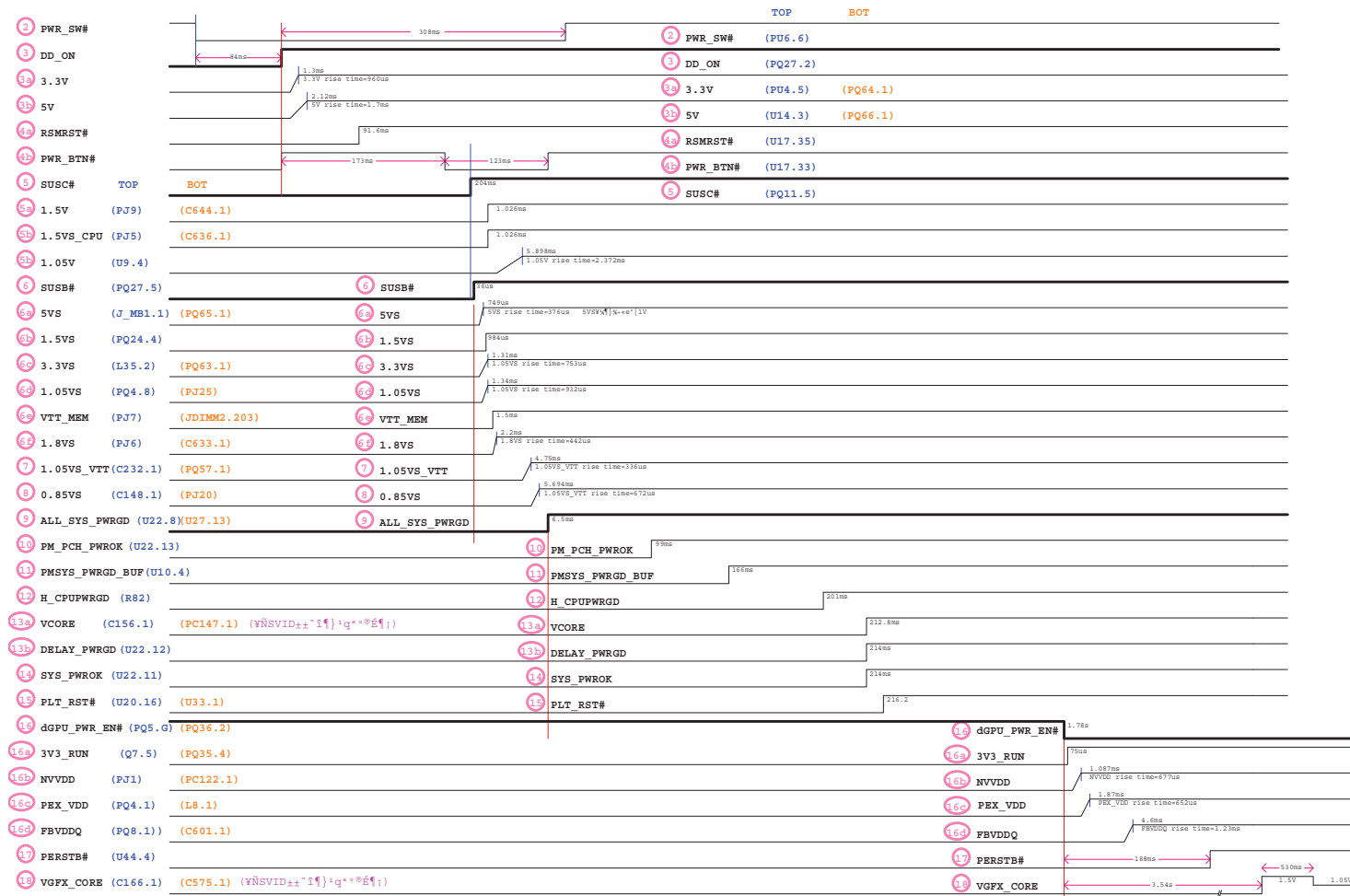
Sheet 48 of 50
W270HU POWER
SW BOARD

Power Diagram

Sheet 49 of 50
Power Diagram



Power On SEQ

Sheet 50 of 50
Power On SEQ

Appendix C: Updating the FLASH ROM BIOS

To update the FLASH ROM BIOS, you must:

- Download the BIOS update from the web site.
- Unzip the files onto a bootable CD/DVD/USB Flash Drive.
- Reboot your computer from an external CD/DVD/USB Flash Drive.
- Use the flash tools to update the flash BIOS using the commands indicated below.
- Restart the computer booting from the HDD and press **F2** at startup enter the BIOS.
- Load setup defaults from the BIOS and save the default settings and exit the BIOS to restart the computer.
- After rebooting the computer you may restart the computer again and make any required changes to the default BIOS settings.

Download the BIOS

1. Go to www.clevo.com.tw and point to **E-Services** and click **E-Channel**.
2. Use your user ID and password to access the appropriate download area (BIOS), and download the latest BIOS files (the BIOS file will be contained in a batch file that may be run directly once unzipped) for your computer model (see sidebar for important information on BIOS versions).

Unzip the downloaded files to a bootable CD/DVD/ or USB Flash drive

1. Insert a bootable CD/DVD/USB flash drive into the CD/DVD drive/USB port of the computer containing the downloaded files.
2. Use a tool such as Winzip or Winrar to unzip all the BIOS files and refresh tools to your bootable CD/DVD/USB flash drive (you may need to create a bootable CD/DVD with the files using a 3rd party software).

Set the computer to boot from the external drive

1. With the bootable CD/DVD/USB flash drive containing the BIOS files in your CD/DVD drive/USB port, restart the computer and press **F2** (in most cases) to enter the BIOS.
2. Use the arrow keys to highlight the **Boot** menu.
3. Use the “+” and “-” keys to move boot devices up and down the priority order.
4. Make sure that the CD/DVD drive/USB flash drive is set first in the boot priority of the BIOS.
5. Press **F4** to save any changes you have made and exit the BIOS to restart the computer.



BIOS Version

Make sure you download the latest correct version of the BIOS appropriate for the computer model you are working on.

You should only download BIOS versions that are **V1.01.XX or higher** as appropriate for your computer model.

Note that BIOS versions are not backward compatible and therefore **you may not downgrade your BIOS to an older version** after upgrading to a later version (e.g if you upgrade a BIOS to ver 1.01.05, you **MAY NOT** then go back and flash the BIOS to ver 1.01.04).

BIOS Update

Use the flash tools to update the BIOS

1. Make sure you are not loading any memory management programs such as HIMEM by holding the **F8** key as you see the message “**Starting MS-DOS**”. You will then be prompted to give “**Y**” or “**N**” responses to the programs being loaded by DOS. Choose “**N**” for any memory management programs.
2. You should now be at the DOS prompt e.g: **DISK C:\>** (C is the designated drive letter for the CD/DVD drive/USB flash drive).
3. **Type the following command** at the DOS prompt:

C:\> Flash.bat

4. The utility will then proceed to flash the BIOS.
5. You should then be prompted to press any key to restart the system or turn the power off, and then on again but make sure you remove the CD/DVD/USB flash drive from the CD/DVD drive/USB port before the computer restarts.

Restart the computer (booting from the HDD)

1. With the CD/DVD/USB flash drive removed from the CD/DVD drive/USB port the computer should restart from the HDD.
2. Press **F2** as the computer restarts to enter the BIOS.
3. Use the arrow keys to highlight the **Exit** menu.
4. Select **Load Setup Defaults** (or press **F3**) and select “**Yes**” to confirm the selection.
5. Press **F4** to save any changes you have made and exit the BIOS to restart the computer.

Your computer is now running normally with the updated BIOS

You may now enter the BIOS and make any changes you require to the default settings.