1.HSIC1_WLAN2SOC_DEVICE_RDY
2.PMU_GPIO_BT_REG_ON_R
3.PMU_GPIO_WLAN_REG_ON_R
4.PMU_GPIO_BT_REG_ON
5.PMU_GPIO_WLAN_REG_ON
6.JTAG_WLAN_TMS_TX_BLANK
7.JTAG_WLAN_TDI_OSCAR_A
8.HSIC1_SOC2WLAN_HOST_RDY_R
9.JTAG_WLAN_SEL
10.TP_JTAG_WLAN_TCK
11.TP_JTAG_WLAN_TRST_L
12.JTAG_WLAN_TDO_OSCAR_B
13.OSCAR2RADIO_CONTEXT_A
14.PMU_GPIO_WLAN_HOST_WAKE
15.VCC_MAIN_GRAPE_RAMP
16.WLAN_TX_BLANK
17.PP3V3_S2R
18.GPIO_BT_WAKE
19.SIM_TRAY_DETECT
20.UART2_SOC2WLAN_TX_R
21.SIMCRD_CLK_CONN_FILT
22. UART2_WLAN2SOC_TX_R
23.UART_BB2WLAN_LTE_COEX_R
24.UART_WLAN2BB_LTE_COEX_R
25.BOARD_TEMP3_P
26.SIMCRD_CLK_CONN

1.PMU_GPIO_CLK_32K_WLAN_R
2.UART1_BT2SOC_RTS_L
3.UART1_BT2SOC_TX
4.UART1_SOC2BT_RTS_L
5&12&15&17&21&26&28.GND
6.GPIO_SOC2GRAPE_RESET_L

7.CUMULUS_M_VDDCORE
8.CUMULUS_M_VDDANA
9. CUMULUS_S_VDDCORE
10.TP_CUMULUS_S_H_SDO
11.TP_CUMULUS_S_H_SDI
13.CUMULUS_MS_CK
14.CUMULUS_S_BCFG_RTCK
16.JTAG_CUMULUS_S_TMS
18.CUMULUS_MS_SD
19.TP_CUMULUS_S_H_SCLK
20.CUMULUS_S_VDDANA
22.PP5V25_GRAPE
23.TP_CUMULUS_S_H_CS_L
24.GPIO_GRAPE2SOC_IRQ_L
25.PP1V8_GRAPE_SW
27.DISPLAY_SYNC
29.CUMULUS_M_BCFG_RTCK
30.SPI2_GRAPE_MOSI
31.TP_JTAG_CUMULUS_M_TDI
32.TP_JTAG_CUMULUS_M_TDO
33.SPI2_GRAPE_CS_L
34.TP_JTAG_CUMULUS_M_TCK
35.SPI2_GRAPE_SCLK
36.JTAG_CUMULUS_M_TMS

1&19&20&22&24&25&26&27&28&29&30&31&32&33.GND
2.PP1V8_SW1_FOREHEAD
3.PP_RF1_1V8_DIG
4.GPIO_SOC2BB_WAKE_MODEM
5.HSIC2_SOC2BB_HOST_RDY
6.PS_HOLD_PMIC
7.BB_JTAG_TMS
8.DEBUG_RST_L
9.USB_BB_DEBUG_N
10.USB_BB_DEBUG_P
11.BB_JTAG_TRST_L
12.BB_JTAG_TCK
13.BB_JTAG_TDI
14.BB_JTAG_TDO
15.BB_JTAG_RTCLK
16.PP_SMPS1_MSMC_1V05
17.PP_SMPS4_RF2_2V05
18.TP_BB_TEST_MODE_1
21.TP_BB_TEST_MODE_0
23.PP_SMPS2_RF1_1V3

1&2&4&5&6.GND
3.PP3V0_SENSOR_PROX_AD7149_FILT
7.PP2V9_AVDD_CAM_REAR_FILT
8.PP2V6_CAM_REAR_AF_FILT
9.CAM_REAR_VSYNC
10.PP1V8_CAM_REAR_FILT
11.ISP0_CAM_REAR_SHUTDOWN_L_F
12.ISP0_CAM_REAR_SDA_F
13.PP1V3_CAM_REAR_FILT
14.ISP0_CAM_REAR_CLK_F
15.ISP0_CAM_REAR_SCL_F
16.PP1V8_S2R_SW3_COMP

1.SIM_TRAY_DETECT_FILT
2.SIMCRD_RST_CONN_FILT
3.PP3V0_S2R_NAVAJO_FILT
4&5&6.PPVBUS_E75_USB_CONN
7.PMU_GPIO_MB_HALL1_IRQ
8.SIMCRD_IO_CONN_FILT
9.PP_LDO6_RUIM_1V8_FILT
10.PMU_GPIO_MB_HALL2_IRQ_FILT
11&12&13&14&60.GND
15.MAX983X4_L1_GAIN
16.PMU_GPIO_MB_HALL2_IRQ
17.SPKRAMP_L1_OUT_P
18.LEFT_CH_OUT_N
19.LEFT_CH_OUT_P
20.SPKRAMP_L1_OUT_N
21.MAX983X4_L2_GAIN
22.AUD_SPKRAMP_MUTE_L
23.RIGHT_CH_OUT_N
24.RIGHT_CH_OUT_P
25.PPOUT_E75_ACC_ID1_CONN
26.SPKRAMP_L2_OUT_N
27.SPKRAMP_L2_OUT_P
28.PPOUT_E75_ACC_ID2_CONN
29.E75_DPAIR2_CONN_N
30.E75_DPAIR2_CONN_P
31.SPKRAMP_R2_OUT_P
32.MAX983X4_R1_GAIN
33.SPKRAMP_R1_OUT_P
34.SPKRAMP_R1_OUT_N
35.MAX983X4_R2_GAIN
36.SPKRAMP_R2_OUT_N
37.E75_ACC_DET_CONN_L
38.E75_DPAIR1_CONN_N
39.E75_DPAIR1_CONN_P
40.LED_IO_1_B
41.LED_IO_2_B
42.LED_IO_4_B
43.LED_IO_3_B
44.LED_IO_6_A
45.LED_IO_5_B
46.LED_IO_6_B
47.LED_IO_5_A
48.LED_IO_4_A
49.LED_IO_3_A
50.PPVCC_MAIN_LCD_SW_CONN
51.PPVCC_MAIN_LCD_SW
52.CLK_32K_SOC2CUMULUS
53.LED_IO_2_A
54.LED_IO_1_A
55.EDP_HPD_EMI_CONN
56.PPLED_BACK_REG_A
57.PPLED_BACK_REG_B
58.PPLED_OUT_A
59.PP1V8_SW2
61.PP3V3_ACC
62.PMU_USB_BRICKID
63.RESET_SOC_L
64.UART0_SOC_RXD
65.USB_SOC_P
66.USB_SOC_N
67.JTAG_SOC_TCK
68.USB_BB_P
69.TS_E75_ACC_DET_L
70.JTAG_SOC_TMS
71.USB_BB_N
72.PMU_E75_ACC_DET_L

1.FMI0_CLE
2. BOARD_TEMP5_P
3.GPIO_BTN_HOME_L
4.PPVREF_FMI_NAND
5.PP1V8_EXT_SW
6.FMI0_RE_L
7.FMI0_CE0_L
8.FMI0_WE_L
9. FMI0_ALE
10.FMI0_AD<7>
11.FMI0_DQS
12.FMI0_AD<6>
13.FMI0_AD<5>
14.FMI0_AD<4>
15.FMI0_AD<0>
16.FMI1_AD<0>
17.FMI0_AD<1>
18.FMI0_AD<2>
19.FMI0_AD<3>
20.PP1V2_S2R
21.PP1V2_SW1
22.PP3V3_SW
23.I2C2_SDA_1V8
24.VCC_MAIN_PP3V3SW_RAMP
25.PP1V8_SW1
26.I2C2_SCL_1V8
27.JTAG_SOC_TDI
28.JTAG_SOC_SEL
29.UART6_TS_ACC_TXD

1.WDOG_SOC
2.SOC_TST_CLKOUT
3.PP1V2_SW1
4.JTAG_SOC_TRST_L
5.TP_JTAG_SOC_TDO
6.PPVREF_FMI_SOC
7&10&11&13&14.GND
8.HSIC1_WLAN2SOC_REMOTE_WAKE
9.UART6_TS_ACC_RXD
12.SOC_TESTMODE
15.UART1_SOC2BT_TX
16.TP_GPIO_DFU_STATUS
17.SPI2_GRAPE_MISO
18.SPI3_CODEC_CS_L
19.GPIO_SOC2PMU_KEEPACT
20.UART0_SOC_TXD
21.WDOG_SOC2PMU_RESET_IN
22.SOC_TST_CPUSWITCH_OUT
23.PMU_GPIO_BT_HOST_WAKE
24.SOCHOT0_L
25.OSCAR_TIME_SYNC_HOST_INT
26.BOARD_TEMP7_P

1.GPIO_TS2SOC2PMU_INT
2.SPI_OSCAR2COMPASS_CS_L
3.GPIO_FORCE_DFU
4.GPIO_SOC2BB_RST_L
5.PMU_GPIO_CLK_32K_OSCAR
6.GPIO_SOC2OSCAR_DBGEN
7.TP_OSCAR_P0_22
8.UART4_SOC2OSCAR_TXD
9.SPI_OSCAR_MISO
10.GPIO_SOC2OSCAR_DBGEN_R
11.PP3V0_S2R_SENSOR
12.PP1V2_S2R_SW2
13.GPIO_BB2SOC_GPS_SYNC
14.OSCAR2RADIO_CONTEXT_B
15.PP1V8_S2R_SW3
16.SOCHOT0_R_L
17.PPVDD_SRAM
18.PP3V0_UVLO
19.PMU_GPIO_OSCAR2PMU_HOST_WAKE
20.PMU_SHDWN
21.PP3V0_S2R_NAVAJO
22.UART4_OSCAR2SOC_RXD
23.PPVDD_SOC
24.ACCEL2OSCAR_INT1
25.GPIO_OSCAR_RESET_L
26.PP2V9_CAM
27.PPVBUS_USB_DCIN
28.PPVDD_GPU
29.DWI_AP_CLK
30.SOCHOT1_L
31.PPVDD_CPU
32.PP1V0_SOC
33.USB_VBUS_DETECT
34.PP1V8_ALWAYS
35.BOARD_TEMP2_P
36.GPIO_PMU2SOC_IRQ_L
37.PP3V0_S2R_TRISTAR
38.PP2V6_CAM_AF
39.VBUS_PROT_G
40.PMU_TCAL
41.PP3V0_ALS
42.PMU_GPIO_PMU2BBPMU_RST_L
43.PPVBUS_PROT
44.BOARD_TEMP8_P
45.PMU_VCENTER
46.BOARD_TEMP6_P
47.TP_HV_CHG_EN
48.PPVCC_MAIN
49.TP_AMUX_B3
50.TP_AMUX_BY
51.TP_AMUX_AY
52.TP_AMUX_A3
53.DWI_AP_DO
54.PP1V3_CAM
55. I2C0_SCL_1V8
56. I2C0_SDA_1V8

1.GPIO_SOC2BB_WAKE_MODEM
2.GPIO_BTN_VOL_UP_L
3.GYRO2OSCAR_INT2
4.GPIO_BTN_VOL_DOWN_L
5.GPIO_BTN_SRL_L_FILT
6.PP3V0_GYRO
7.SPI_OSCAR2GYRO_CS_L
8.GPIO_BTN_VOL_UP_L_FILT
9.SIMCRD_IO_CONN
10.SIMCRD_RST_CONN
11.GPIO_BTN_ONOFF_L_FILT
12.GPIO_BTN_VOL_DOWN_L_FILT
13.GPIO_HS4_SHUNT_EN
14.PP3V0_SPARE1
15.PP6V0_LCM_VBOOST
16.GPIO_BB2SOC_RESET_DET_L
17.UART_WLAN2BB_LTE_COEX
18&58.BATT_NTC
19.GPIO_SOC2BB_RADIO_ON_L
20.GPIO_BTN_SRL_L
21.GPIO_BTN_ONOFF_L
22.PA_NTC_P
23.PP_LDO6_RUIM_1V8
24.GPIO_CODEC2SOC_IRQ_L
25.SPI3_CODEC_MISO
26.SPI3_CODEC_SCLK
27.GPIO_BB2SOC_GSM_TXBURST
28.ACCEL2OSCAR_INT2
29.GYRO2OSCAR_INT1
30.GYRO_DEN
31.SPI_OSCAR2ACCEL_CS_L
32.PP3V0_ACCEL
33.PPBATT_POS_RC
34.AIN3P
35.DMIC1_FF_SCLK
36.AIN3N
37.SPI3_CODEC_MOSI
38.PMU_GPIO_CODEC_HS_INT_L
39.L81_SPEAKER_VQ
40.GND
41.GND_AUDIO_CODEC
42&64&65&66&69.PPBATT_VCC
43&57.BATT_SWI_CONN
44.PMU_GPIO_BB_VBUS_DET
45.PMU_GPIO_BB2PMU_HOST_WAKE
46.PP1V8_S2R
47.PPLED_OUT_B
48.COMPASS2OSCAR_INT
50&51&52&56&59&71&72.GND
53.UART_BB2WLAN_LTE_COEX
54.MIKEY_TS_P
55.MIKEY_TS_N
60.PP1V7_VA_VCP
61.PP1V7_VCP
62.L81_DMIC1_FF_SD
63.CODEC_HP_DET_R
67.GPIO_PROX2SOC_IRQ_L
70.BATT_SNS
73.PP_SMPS5_DSP_1V05
74.PP_LDO1

1.PP3V0_COMP
2.PP3V0_S2R_SENSOR
3.SPI_OSCAR_SCLK
4.SPI_OSCAR_MOSI
5.PP1V8_COMP
6.I2C0_CAM_ALS_SCL_1V8_F
7.GPIO_CAM_ALS2SOC_IRQ_L_F
8.ISP1_CAM_FRONT_SDA_F
9.ISP1_CAM_FRONT_SCL_F
10.PP3V0_ALS_FILT
11.I2C0_CAM_ALS_SDA_1V8_F
12.ISP1_CAM_FRONT_CLK_F
13.ISP1_CAM_FRONT_SHUTDOWN_L_F
14.PP2V9_AVDD_CAM_FRONT_FILT
15.PP1V8_CAM_FRONT_FILT
16.GPIO_HS3_SHUNT_EN_FILT
17.CONN_HP_HEADSET_DET_FILT
18.GPIO_HS4_SHUNT_EN_FILT
19.CONN_HP_HS4_REF_FILT
20.CONN_HP_HS3_FILT
21.CONN_HP_RIGHT_FILT
22.CONN_HP_LEFT_FILT
23. CONN_HP_HS4_FILT
24.CONN_HP_HS3_REF_FILT
25.BOARD_TEMP4_P
26.DMIC1_FF_SCLK_FILT
27.DMIC1_FF_SD
28.DMIC1_FF_SD_FILT
29.PP1V8_DMIC_FILT
30. GPIO_HS3_SHUNT_EN

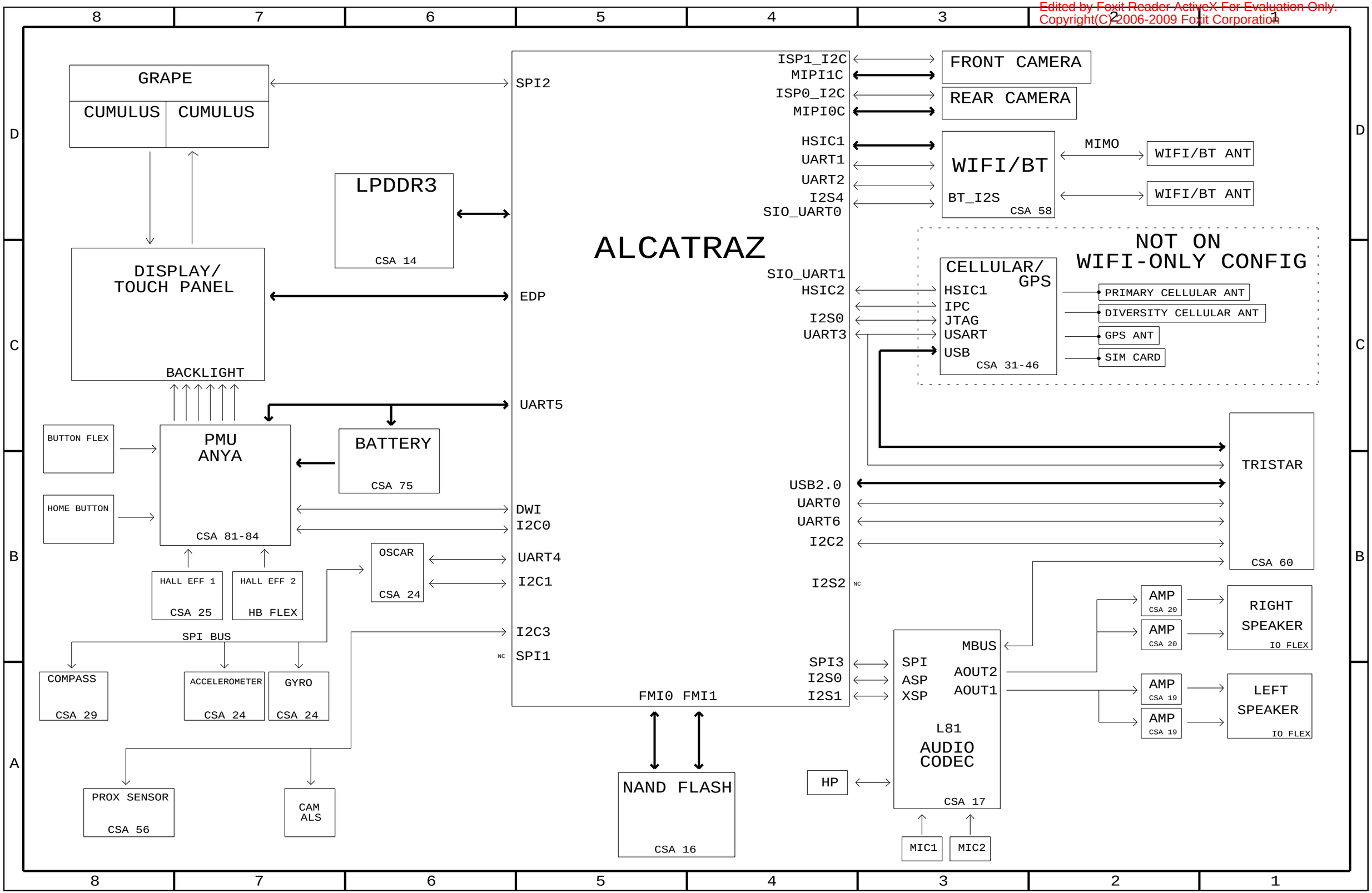
J6200

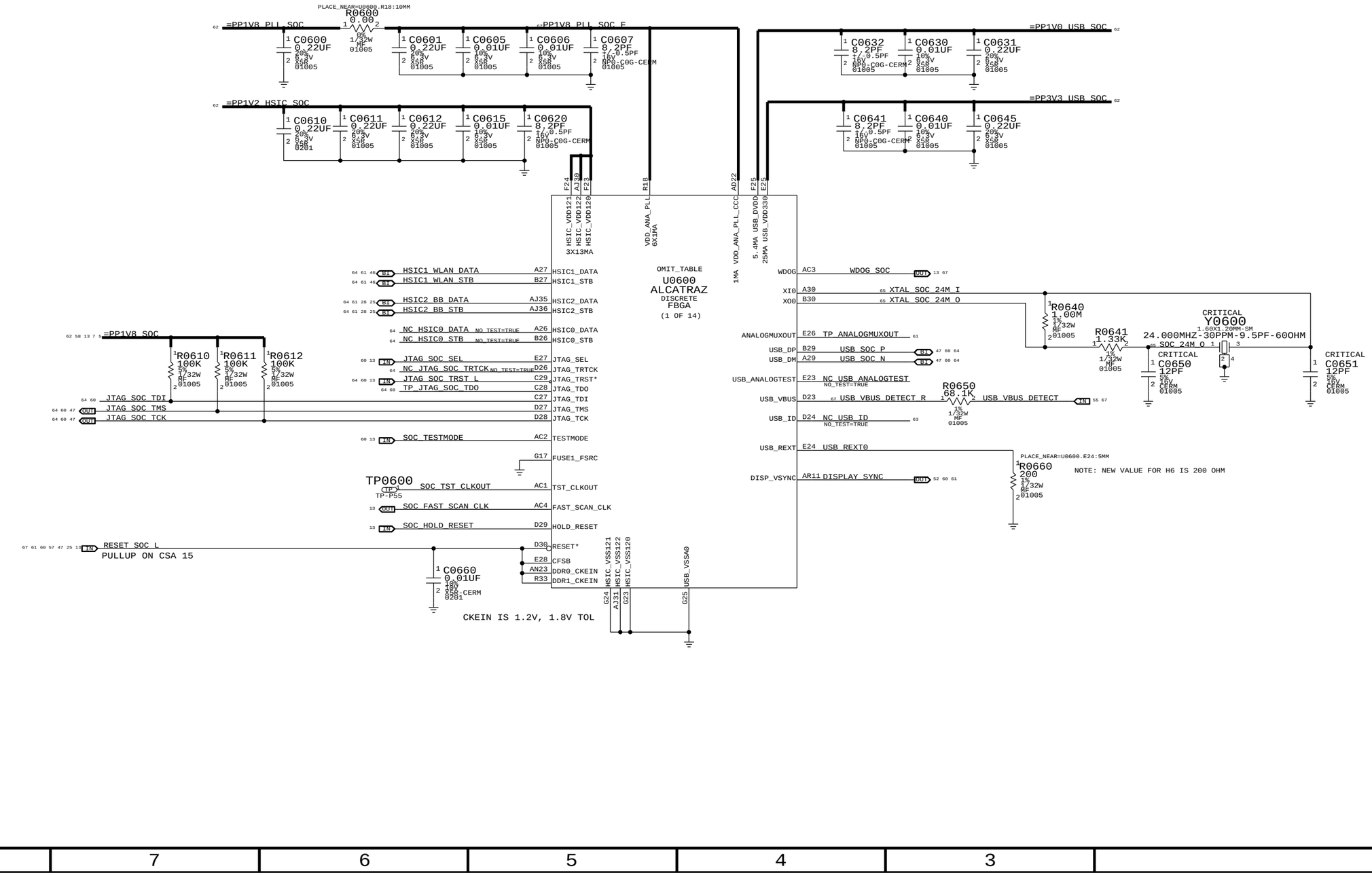
J3002

J3001

J3003

R4802 C4802 C4801 R4801





I2S0 AND I2S2 ARE OPTIMIZED FOR LOW MCK JITTER

R0700 33 2 1/32W MF 01005

64 15 OUT I2S0_CODEC_ASP_MCK_R 1

L81 CODEC ASP 1.8V

64 I2S0_CODEC_ASP_MCK F28 I2S0_MCK
64 15 OUT I2S0_CODEC_ASP_BCLK AJ32 I2S0_BCLK
64 15 OUT I2S0_CODEC_ASP_LRCK AH32 I2S0_LRCK
64 15 IN I2S0_CODEC_ASP_DIN AG32 I2S0_DIN
64 15 OUT I2S0_CODEC_ASP_DOUT AJ33 I2S0_DOUT

L81 CODEC XSP 1.8V

64 NC_I2S1_MCK NO_TEST=TRUE AG33 I2S1_MCK
64 15 OUT I2S1_CODEC_XSP_BCLK AH34 I2S1_BCLK
64 15 OUT I2S1_CODEC_XSP_LRCK AH33 I2S1_LRCK
64 15 IN I2S1_CODEC_XSP_DIN AG34 I2S1_DIN
64 15 OUT I2S1_CODEC_XSP_DOUT AF32 I2S1_DOUT

UNUSED 1.8V

64 NC_I2S2_MCK NO_TEST=TRUE F26 I2S2_MCK
64 NC_I2S2_BCLK NO_TEST=TRUE AG35 I2S2_BCLK
64 NC_I2S2_LRCK NO_TEST=TRUE AE32 I2S2_LRCK
64 NC_I2S2_DIN NO_TEST=TRUE AE33 I2S2_DIN
64 NC_I2S2_DOUT NO_TEST=TRUE AF34 I2S2_DOUT

BT 1.8V

64 61 28 25 OUT BB_JTAG_TRST_L AD32 I2S3_MCK
64 61 28 25 OUT BB_JTAG_TDI AF36 I2S3_BCLK
64 61 28 25 IN BB_JTAG_TDO AG36 I2S3_LRCK
64 61 28 25 OUT BB_JTAG_TCK AC32 I2S3_DIN
64 61 28 25 OUT BB_JTAG_TMS AD33 I2S3_DOUT

64 NC_I2S4_MCK NO_TEST=TRUE AD34 I2S4_MCK
64 46 OUT I2S4_SOC2BT_BCLK AE36 I2S4_BCLK
64 46 OUT I2S4_SOC2BT_LRCK AE35 I2S4_LRCK
64 46 IN I2S4_BT2SOC_DATA AB32 I2S4_DIN
64 46 OUT I2S4_SOC2BT_DATA AC33 I2S4_DOUT

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (3 OF 14)

I2C0_SCL AN6 I2C0_SCL_1V8 OUT 5 57 60 64
I2C0_SDA AP4 I2C0_SDA_1V8 BI 5 57 60 64

I2C1_SCL AP5 I2C1_SOC2OSCAR_SWDCLK_1V8 OUT 5 19 64
I2C1_SDA AR3 I2C1_SOC2OSCAR_SWDIO_1V8 BI 5 19 64

I2C2_SCL AR14 I2C2_SCL_1V8 OUT 5 47 64
I2C2_SDA AT7 I2C2_SDA_1V8 BI 5 47 64

I2C3_SCL AA35 I2C3_SCL_1V8 OUT 5 13 22 61 64
I2C3_SDA AA36 I2C3_SDA_1V8 BI 5 13 22 61 64

DWI_CLK AT17 DWI_AP_CLK OUT 57 64
DWI_DI AT16 SOC_TST_CPUSWITCH_OUT
DWI_DO AR16 DWI_AP_DO OUT 57 64

SEP_7816UART0_RST AL1 NC_SEP_7816UART0_RST NO_TEST=TRUE
SEP_7816UART0_SCL AK5 SEP_I2C0_SCL OUT 5 64
SEP_7816UART0_SDA AK3 SEP_I2C0_SDA BI 5 64
SEP_7816UART1_RST AM1 NC_SEP_7816UART1_RST NO_TEST=TRUE
SEP_7816UART1_SCL AL4 NC_SEP_7816UART1_SCL NO_TEST=TRUE
SEP_7816UART1_SDA AL2 NC_SEP_7816UART1_SDA NO_TEST=TRUE

SIO_7816UART0_RST Y32 HSIC1_WLAN2SOC_REMOTE_WAKE IN 46 61 64
SIO_7816UART0_SCL AB33 HSIC1_WLAN2SOC_DEVICE_RDY IN 46 61 64
SIO_7816UART0_SDA AA32 HSIC1_SOC2WLAN_HOST_RDY OUT 5 46 64
SIO_7816UART1_RST AA34 HSIC2_BB2SOC_REMOTE_WAKE IN 29 64
SIO_7816UART1_SCL AC36 HSIC2_BB2SOC_DEVICE_RDY IN 25 29 64
SIO_7816UART1_SDA AA33 HSIC2_SOC2BB_HOST_RDY OUT 25 29 64

SOCHOT0 AM20 SOCHOT0_L 5 58
SOCHOT1 AM19 SOCHOT1_L OUT 5 57

TO: ANYA PMU 0111100X

TO: OSCAR SWD NOTE: I2C1 IS ASSUMED TO USE PUSH-PULL INSTEAD OF OPEN-DRAIN

TO: TRISTAR 0011010X

TO: AD7149 PROX 0101101X FF CAM CT817 ALS 0111001X

TP0700 1 A TP-P55

60 57 50 5 IN GPIO_BTN_HOME_L AB6 GPIO00
57 21 5 IN GPIO_BTN_ONOFF_L AD1 GPIO01
21 IN GPIO_BTN_VOL_DOWN_L AB5 GPIO02
21 IN GPIO_BTN_VOL_UP_L AC5 GPIO03
22 IN GPIO_CAM_ALS2SOC_IRQ_L AC6 GPIO04
61 46 OUT GPIO_BT_WAKE AD3 GPIO05
29 OUT GPIO_SOC2BB_WAKE_MODEM AD4 GPIO06
NC_GPIO7 NO_TEST=TRUE AE1 GPIO07
67 60 27 25 OUT GPIO_SOC2BB_RST_L AE2 GPIO08
60 27 25 5 OUT GPIO_SOC2BB_RADIO_ON_L AD5 GPIO09
67 29 25 IN GPIO_BB2SOC_RESET_DET_L AF1 GPIO10
NC_GPIO11 NO_TEST=TRUE AF2 GPIO11
19 OUT GPIO_SOC2OSCAR_DBGEN AE4 GPIO12
67 61 60 52 OUT GPIO_SOC2GRAPE_RESET_L AF3 GPIO13
NC_GPIO14 NO_TEST=TRUE AE5 GPIO14
29 IN GPIO_BB2SOC_GSM_TXBURST AE6 GPIO15
13 IN GPIO_BOARD_ID_3 AG1 GPIO16
57 47 IN GPIO_TS2SOC2PMU_INT AF4 GPIO17
13 IN GPIO_BOOT_CONFIG_0 AG3 GPIO18
29 IN GPIO_BB2SOC_GPS_SYNC AF5 GPIO19
13 IN GPIO_PROX2SOC_IRQ_L AH1 GPIO20
53 OUT GPIO_SOC2LCD_PWREN AG4 GPIO21
57 5 OUT GPIO_SOC2PMU_KEEPACT AR10 GPIO22
57 IN GPIO_PMU2SOC_IRQ_L AN14 GPIO23
15 IN GPIO_CODEC2SOC_IRQ_L AR9 GPIO24
13 IN GPIO_BOOT_CONFIG_1 AP13 GPIO25
60 59 5 IN GPIO_FORCE_DFU AT14 GPIO26
61 TP_GPIO_DFU_STATUS AT8 GPIO27
13 IN GPIO_BOOT_CONFIG_2 AM17 GPIO28
13 IN GPIO_BOOT_CONFIG_3 AT9 GPIO29
57 21 5 IN GPIO_BTN_SRL_L AP14 GPIO30
61 60 52 IN GPIO_GRAPE2SOC_IRQ_L AN16 GPIO31
NC_GPIO32 NO_TEST=TRUE AT11 GPIO32
16 OUT GPIO_HS3_SHUNT_EN AT10 GPIO33
16 OUT GPIO_HS4_SHUNT_EN AP11 GPIO34
13 IN GPIO_BRD_REV3 AN17 GPIO35
13 IN GPIO_BRD_REV2 AR13 GPIO36
13 IN GPIO_BRD_REV1 AP16 GPIO37
13 IN GPIO_BRD_REV0 AT13 GPIO38

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (2 OF 14)

TMR32_PWM0 AD35 OSCAR_TIME_SYNC_HOST_INT IN 19
TMR32_PWM1 AC34 NC_TMR32_PWM1 NO_TEST=TRUE
TMR32_PWM2 AD36 CLK_32K_SOC2CUMULUS OUT 52 60 61 64

SOC DEBUG 1.8V

UART0_RXD AR17 UART0_SOC_RXD IN 47 60 64
UART0_TXD AP17 UART0_SOC_TXD OUT 47 60 64

TO BT UART BCM4330

UART1_CTSN AH4 UART1_BT2SOC_RTS_L IN 46 64
UART1_RTSN AH2 UART1_SOC2BT_RTS_L OUT 46 64
UART1_RXD AG6 UART1_BT2SOC_TX IN 46 64
UART1_TXD AG5 UART1_SOC2BT_TX OUT 46 64

WIFI DEBUG

UART2_CTSN AJ3 NC_GPIO_UART2_CTSN NO_TEST=TRUE
UART2_RTSN AH5 NC_GPIO_UART2_RTSN NO_TEST=TRUE
UART2_RXD AJ2 UART2_WLAN2SOC_TX IN 46 64
UART2_TXD AJ1 UART2_SOC2WLAN_TX OUT 46 64

TO BB UART MDM9600

UART3_CTSN AK1 UART3_BB2SOC_RTS_L IN 25 29 64
UART3_RTSN AJ6 UART3_SOC2BB_RTS_L OUT 25 29 64
UART3_RXD AJ5 UART3_BB2SOC_TX IN 25 29 47 64
UART3_TXD AJ4 UART3_SOC2BB_TX OUT 25 29 47 64

TO OSCAR

UART4_CTSN AM3 PMU_GPIO_OSCAR2PMU_HOST_WAKE IN 19 57
UART4_RTSN AM2 GPIO_OSCAR_RESET_L OUT 19 60 67
UART4_RXD AL5 UART4_OSCAR2SOC_RXD IN 19 64
UART4_TXD AL6 UART4_SOC2OSCAR_TXD OUT 19 64

UART5_RTXD AK4 UART5_BATT_TRXD OUT 54 57 64

ACCESSORY UART 1.8V

UART6_RXD AB36 UART6_TS_ACC_RXD IN 47 64
UART6_TXD AB35 UART6_TS_ACC_TXD OUT 47 64

64 15 IN SPI0_CODEC_MISO
64 15 OUT SPI0_CODEC_MOSI
64 15 OUT SPI0_CODEC_SCLK
64 15 OUT SPI0_CODEC_CS_L

13 IN GPIO_BOARD_ID_2 AN4 SPI0_MISO
13 IN GPIO_BOARD_ID_1 AP2 SPI0_MOSI
13 IN GPIO_BOARD_ID_0 AN3 SPI0_SCLK
NC_SPI0_SSIN NO_TEST=TRUE AM9 SPI0_SSIN

NC_SPI1_MISO NO_TEST=TRUE AN1 SPI1_MISO
NC_SPI1_MOSI NO_TEST=TRUE AM4 SPI1_MOSI
NC_SPI1_SCLK NO_TEST=TRUE AM5 SPI1_SCLK
NC_SPI1_SSIN NO_TEST=TRUE AM7 SPI1_SSIN

64 61 60 52 IN SPI2_GRAPE_MISO AN8 SPI2_MISO
64 61 60 52 OUT SPI2_GRAPE_MOSI AN7 SPI2_MOSI
64 61 60 52 OUT SPI2_GRAPE_SCLK AN5 SPI2_SCLK
64 61 60 52 OUT SPI2_GRAPE_CS_L AN9 SPI2_SSIN

64 15 IN SPI3_CODEC_MISO AN13 SPI3_MISO
64 15 OUT SPI3_CODEC_MOSI AT6 SPI3_MOSI
64 15 OUT SPI3_CODEC_SCLK AR7 SPI3_SCLK
64 15 OUT SPI3_CODEC_CS_L AP10 SPI3_SSIN

BUTTON PULLUPS

62 =PP1V8_ALWAYS
62 59 5 =PP1V8_S2R_MISC

R0722 100K 5% 1/32W MF 01005
R0720 100K 5% 1/32W MF 01005
NOSTUFF R0723 100K 5% 1/32W MF 01005
R0721 100K 5% 1/32W MF 01005

57 21 5 GPIO_BTN_SRL_L
60 57 50 5 GPIO_BTN_HOME_L
57 21 5 GPIO_BTN_ONOFF_L

=PP1V8_S2R_MISC 5 59 62
=PP1V8_SOC 4 5 7 13 58 62

R0760 100K 5% 1/32W MF 01005
R0761 100K 5% 1/32W MF 01005

57 5 SOCHOT1_L
58 5 SOCHOT0_L

GPIO_SOC2PMU_KEEPACT 5 57
GPIO_FORCE_DFU 5 59 60
GPIO_SOC2BB_RADIO_ON_L 5 25 27 60
HSIC1_SOC2WLAN_HOST_RDY 5 46 64

R0730 100K 5% 1/32W MF 01005
R0731 100K 5% 1/20W MF 0201
NOSTUFF R0733 100K 5% 1/32W MF 01005
R0734 100K 5% 1/32W MF 01005

SEP EEPROM

UNPROGRAMMED P/N: 335S0894

=PP1V8_EEPROM 62
C9000 0.22UF 20% 6.3V X5R 01005

CRITICAL U9000 CAT24C08C4A WLCSP

A1 VCC
B1 SCL
B2 SDA
VSS A2

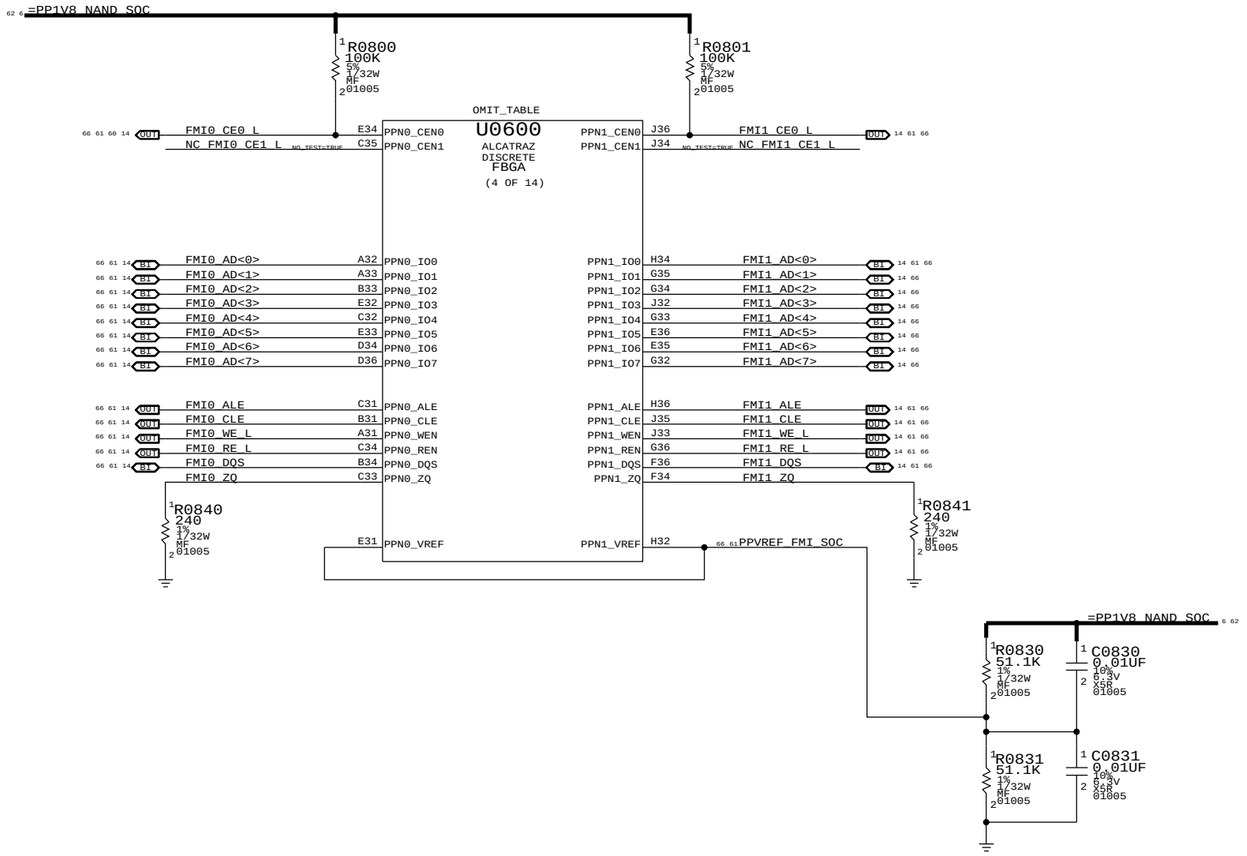
64 5 SEP_I2C0_SCL
SEP_I2C0_SDA 5 64

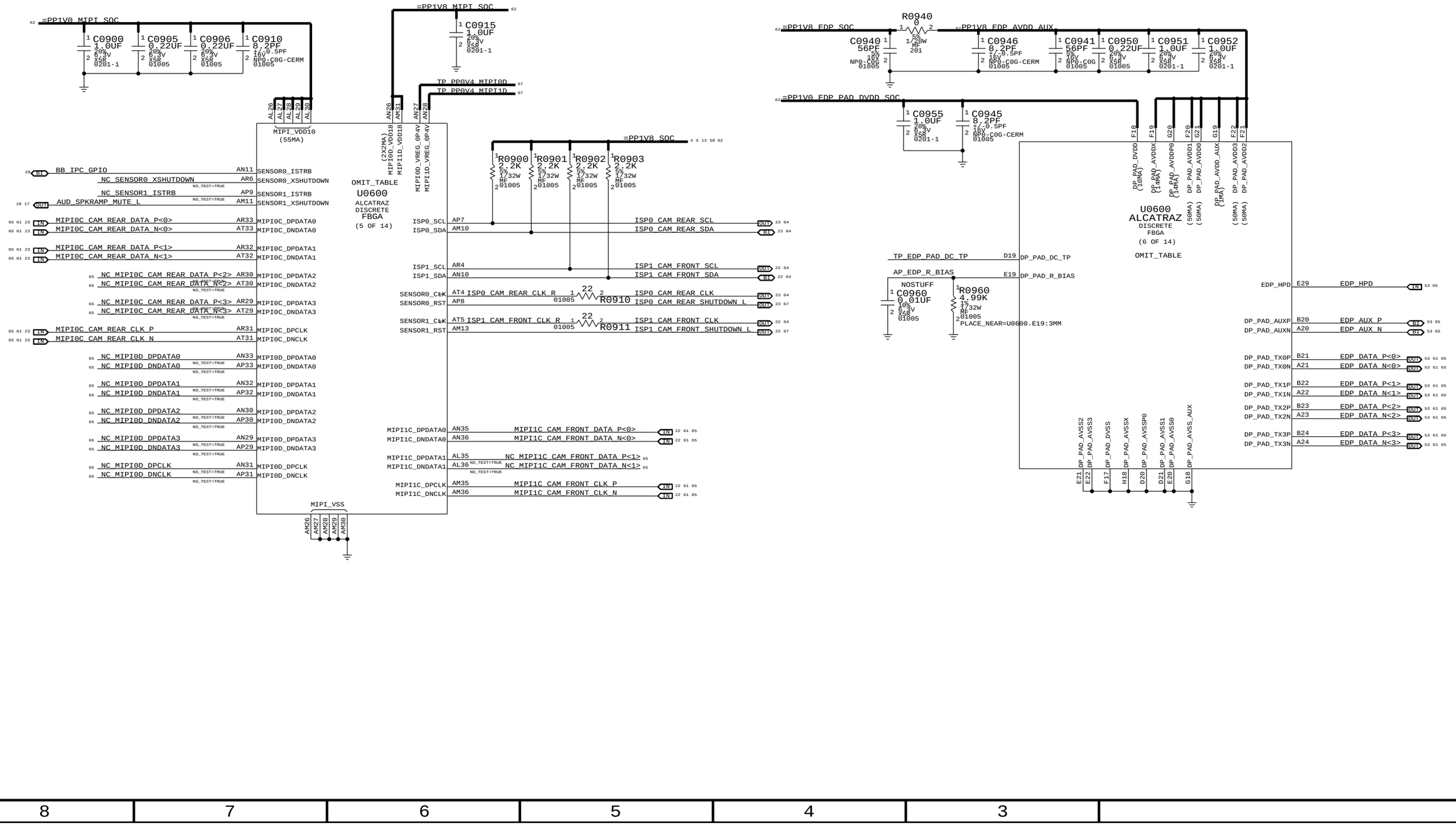
I2C PULL-UPS

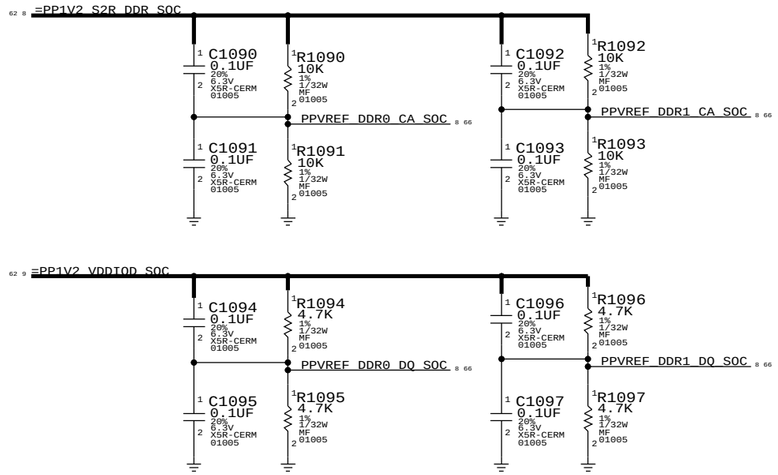
62 58 13 7 5 4 =PP1V8_SOC

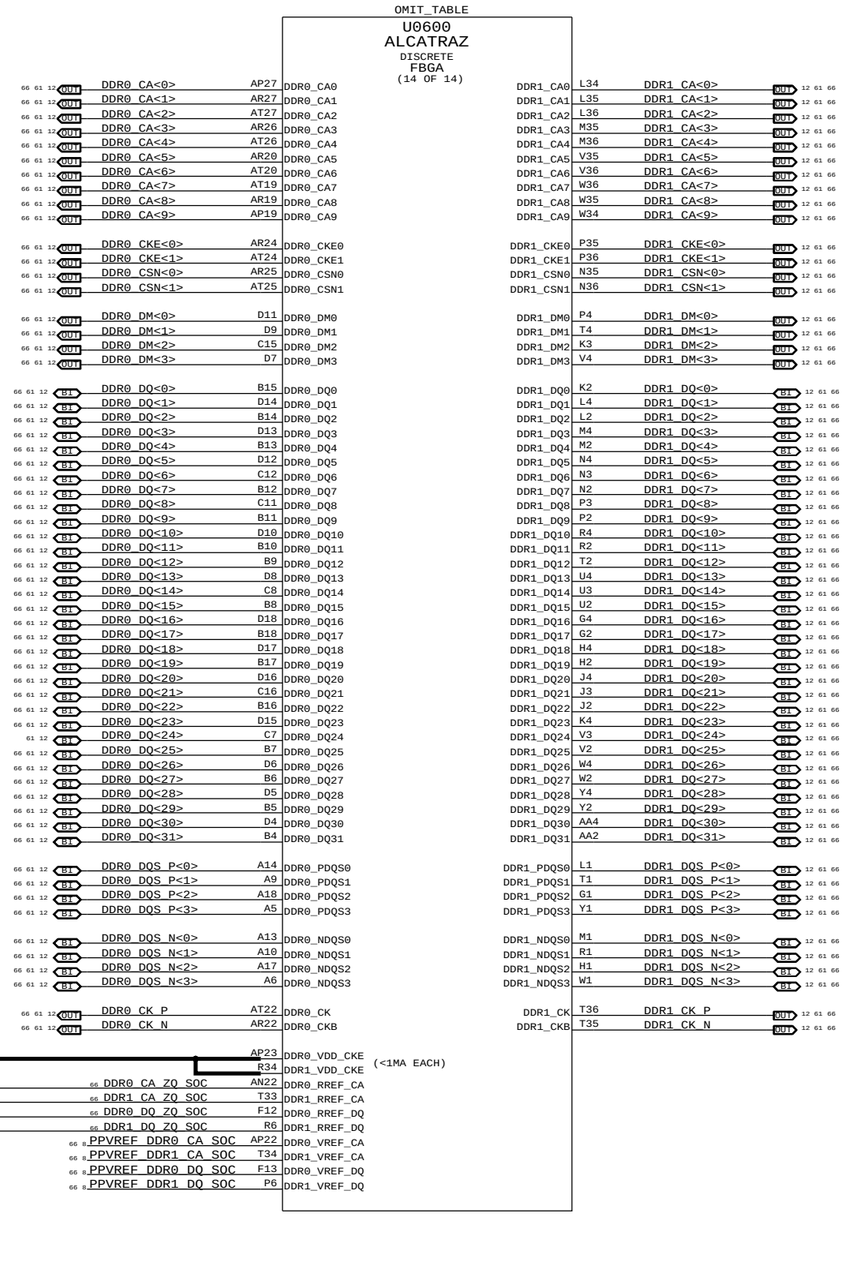
R0750 2.2K 5% 1/32W MF 01005
R0751 2.2K 5% 1/32W MF 01005
R0752 2.2K 5% 1/32W MF 01005
R0753 2.2K 5% 1/32W MF 01005
R0754 2.2K 5% 1/32W MF 01005
R0755 2.2K 5% 1/32W MF 01005
R0756 2.2K 5% 1/32W MF 01005
R0757 2.2K 5% 1/32W MF 01005
NOSTUFF R0758 2.2K 5% 1/32W MF 01005
NOSTUFF R0759 2.2K 5% 1/32W MF 01005

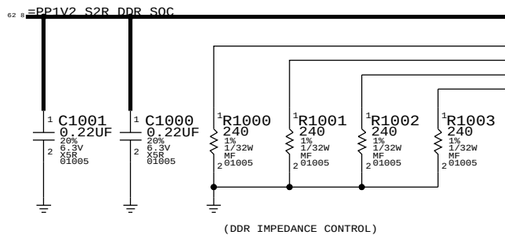
64 60 57 5 I2C0_SDA_1V8
64 60 57 5 I2C0_SCL_1V8
64 61 22 13 5 I2C3_SDA_1V8
64 61 22 13 5 I2C3_SCL_1V8
64 47 5 I2C2_SDA_1V8
64 47 5 I2C2_SCL_1V8
64 5 SEP_I2C0_SDA
64 5 SEP_I2C0_SCL
64 19 5 I2C1_SOC2OSCAR_SWDCLK_1V8
64 19 5 I2C1_SOC2OSCAR_SWDIO_1V8

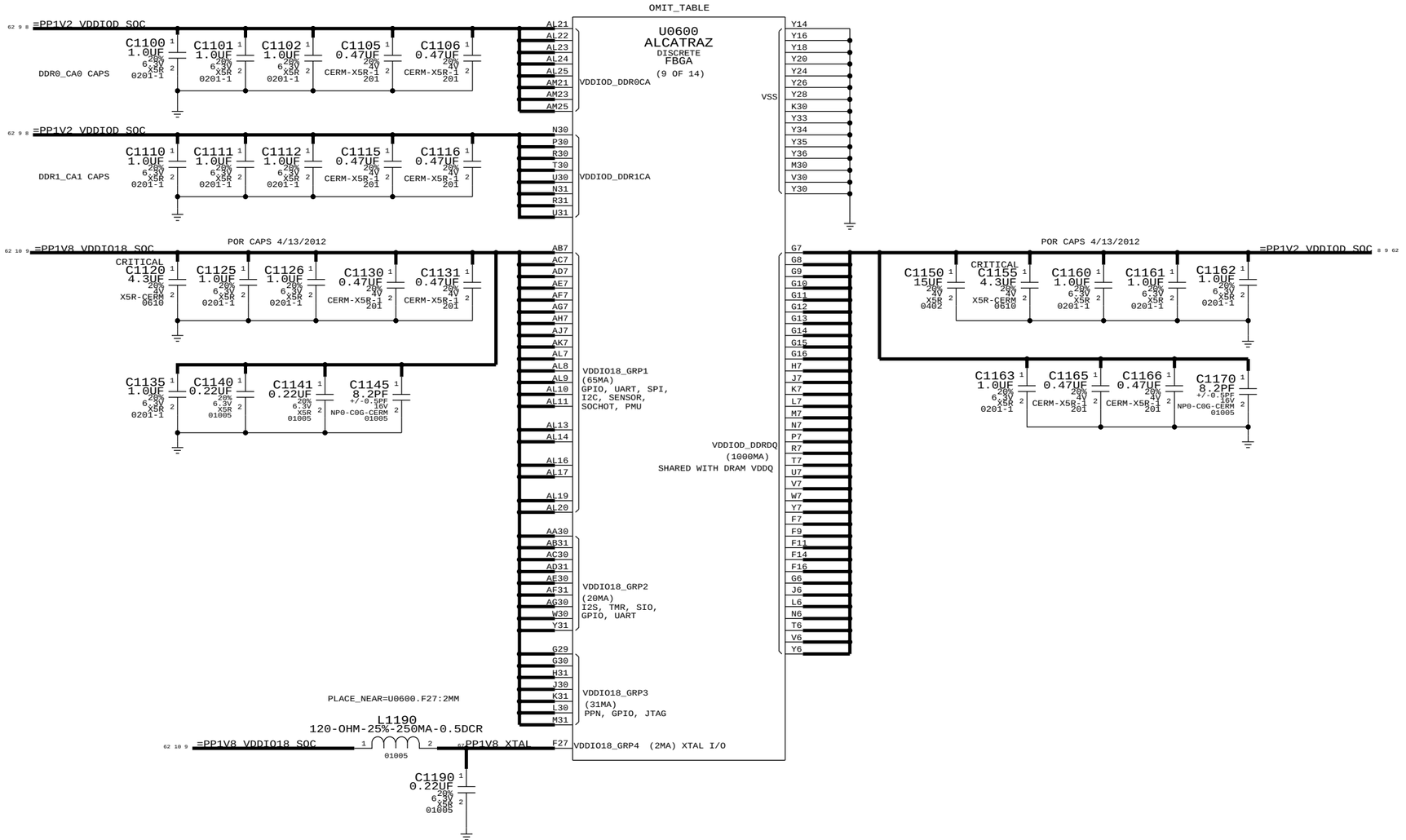


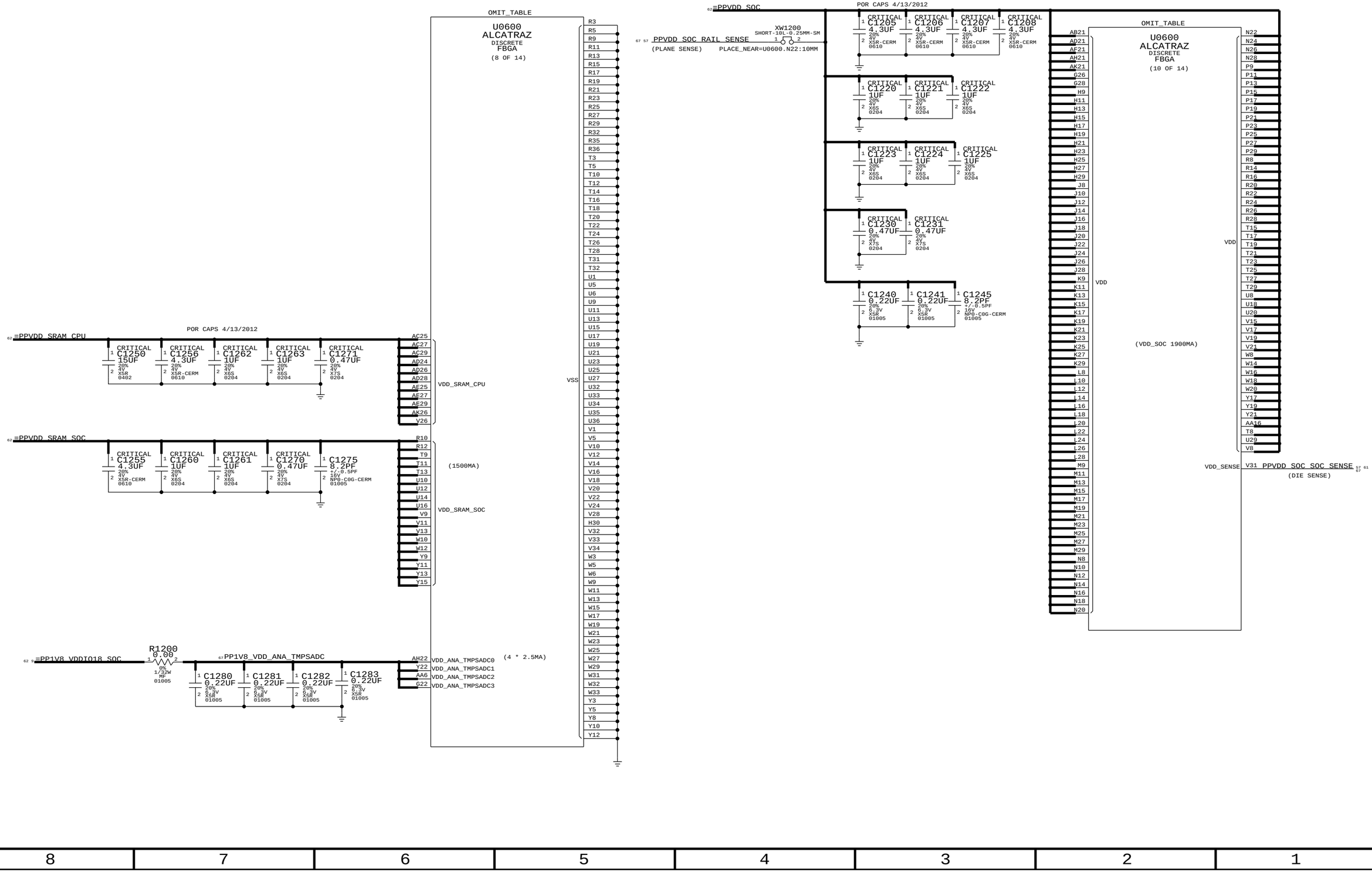


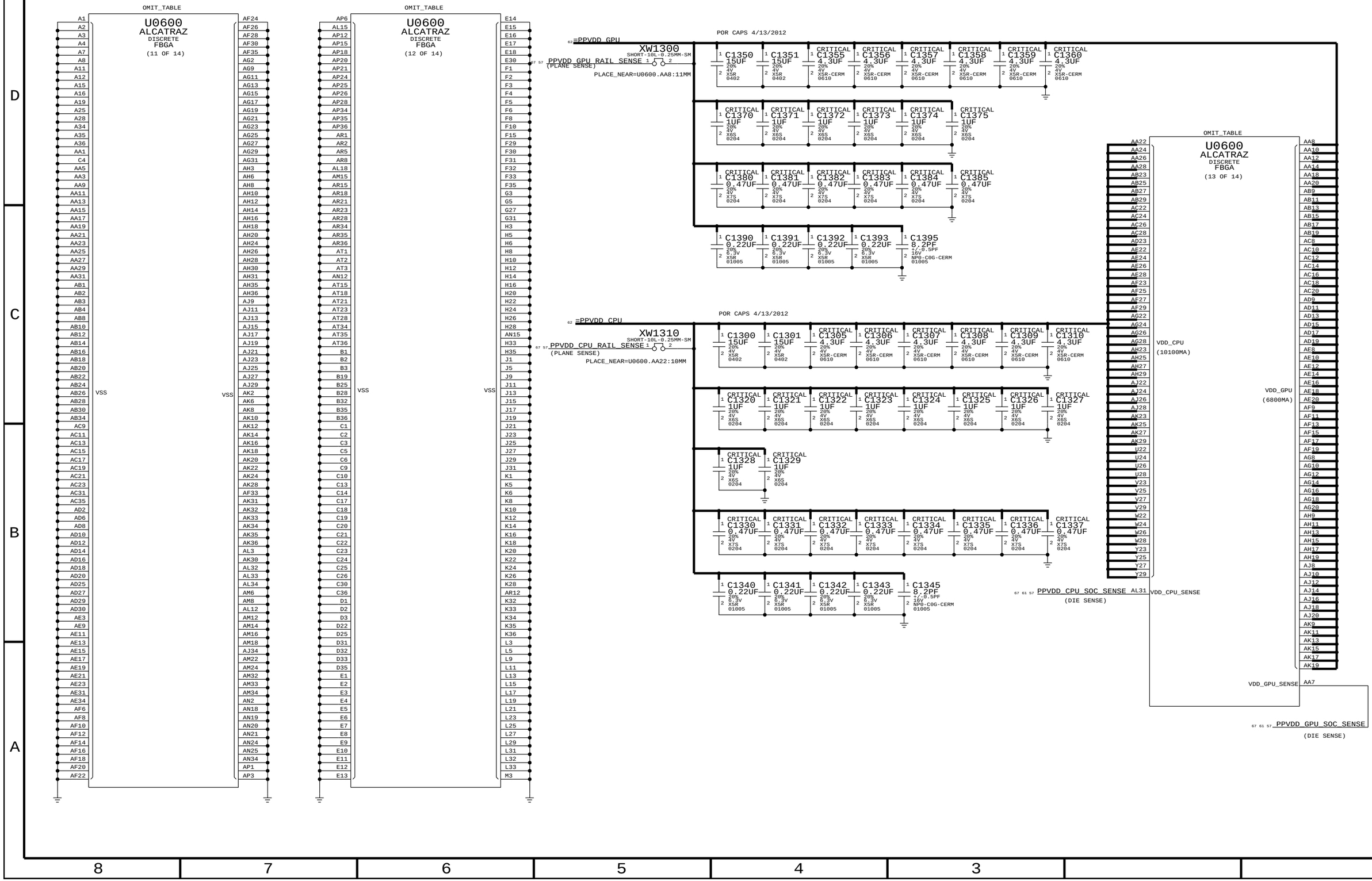


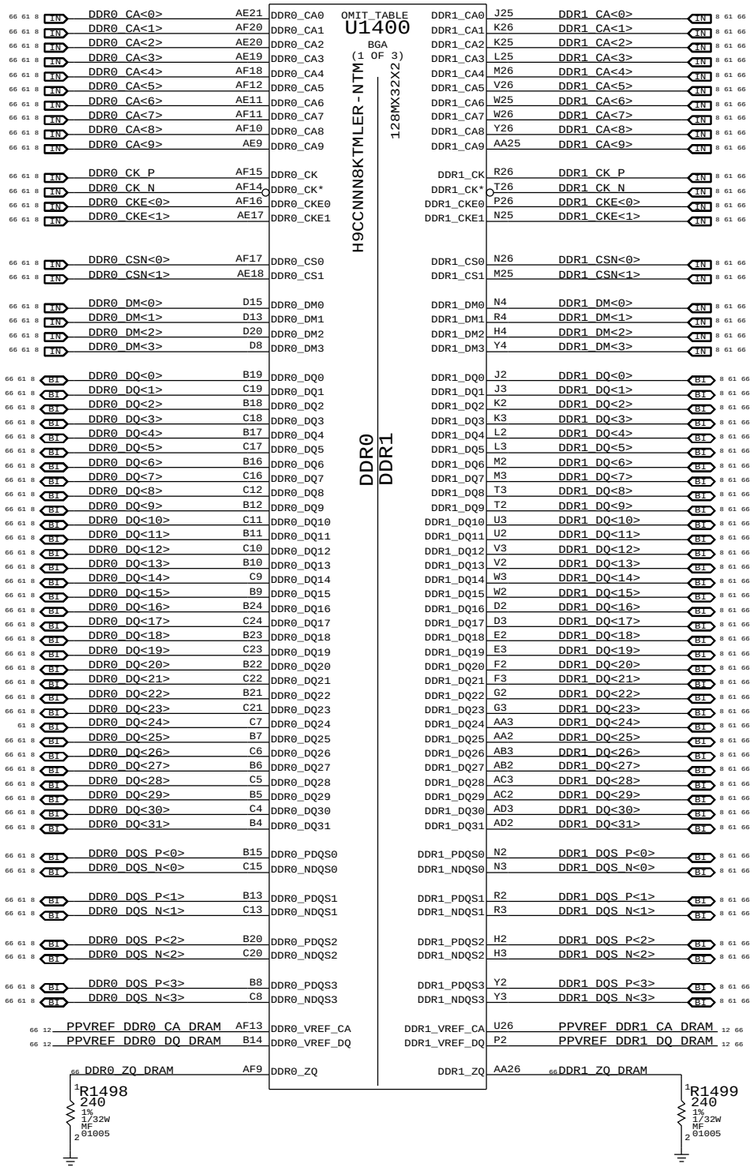


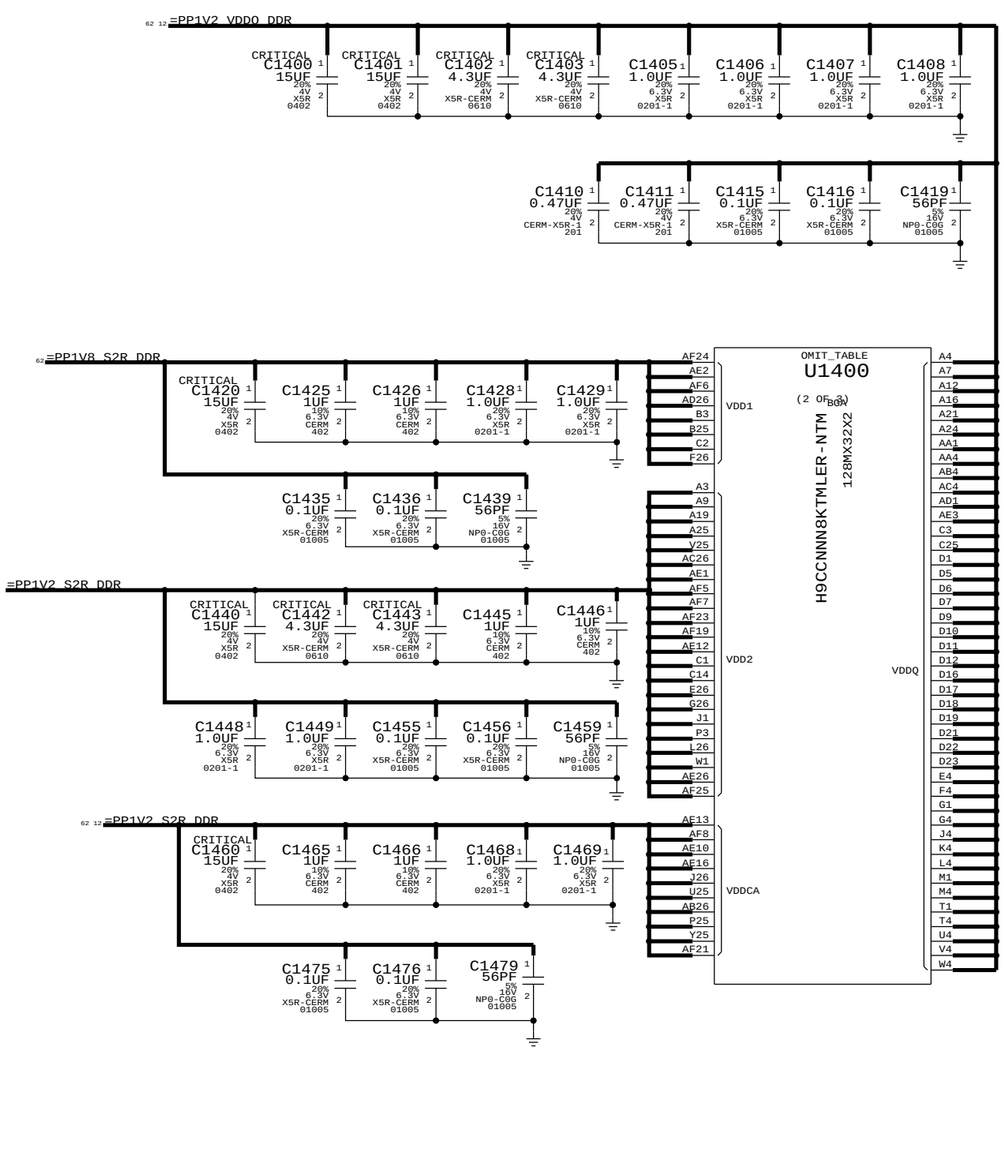


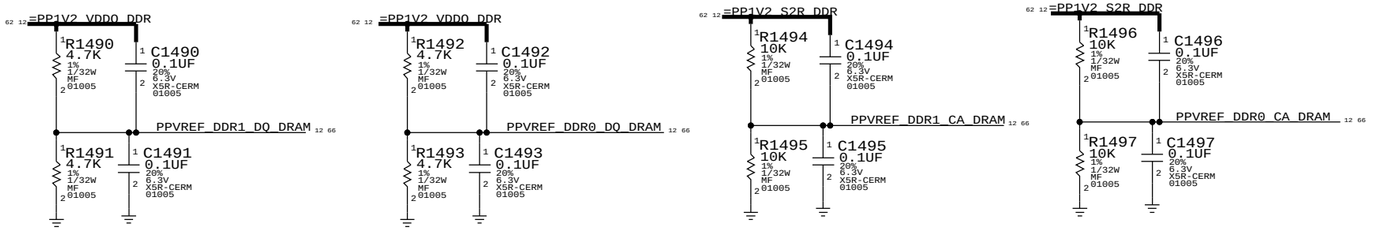




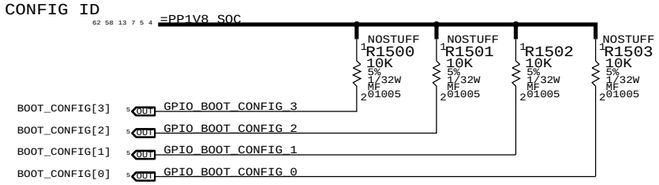








BOOT CONFIG ID

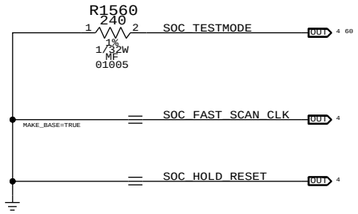


BOOT_CONFIG[3:0]	MODE
0000	SPI
0001	SPI W/TEST
0010	NAND <-- CURRENT SETTING
0011	NAND W/TEST

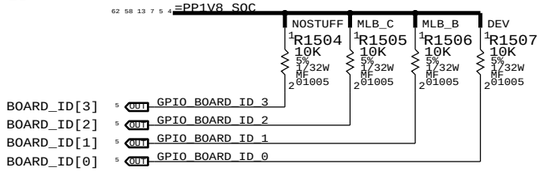
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

JTAG



BOARD ID

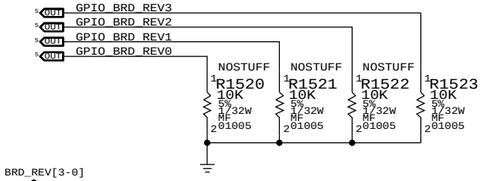


BOARD_ID[3-0]	
0000	MLB_A AP
0001	MLB_A DEV
0010	MLB_B AP
0011	MLB_B DEV
0100	MLB_C AP
0101	MLB_C DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

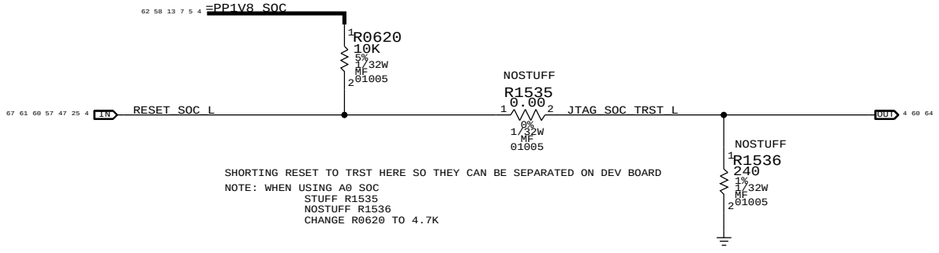
BOARD REVISION



BRD_REV[3-0]	
0000	PROTO 0
0001	PROTO 0 + T2
0010	PROTO 1 + T2
0011	PROTO 1 + T1
0100	PROTO 1 + T1 + B0
0101	PROTO 2 + T2 + B0
0110	EVT + T2 + B0
CURRENT SETTING ---> 0111	DVT + T2 + B1

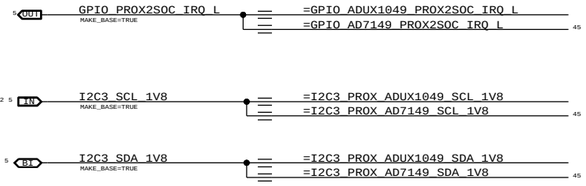
S/W READ FLOW

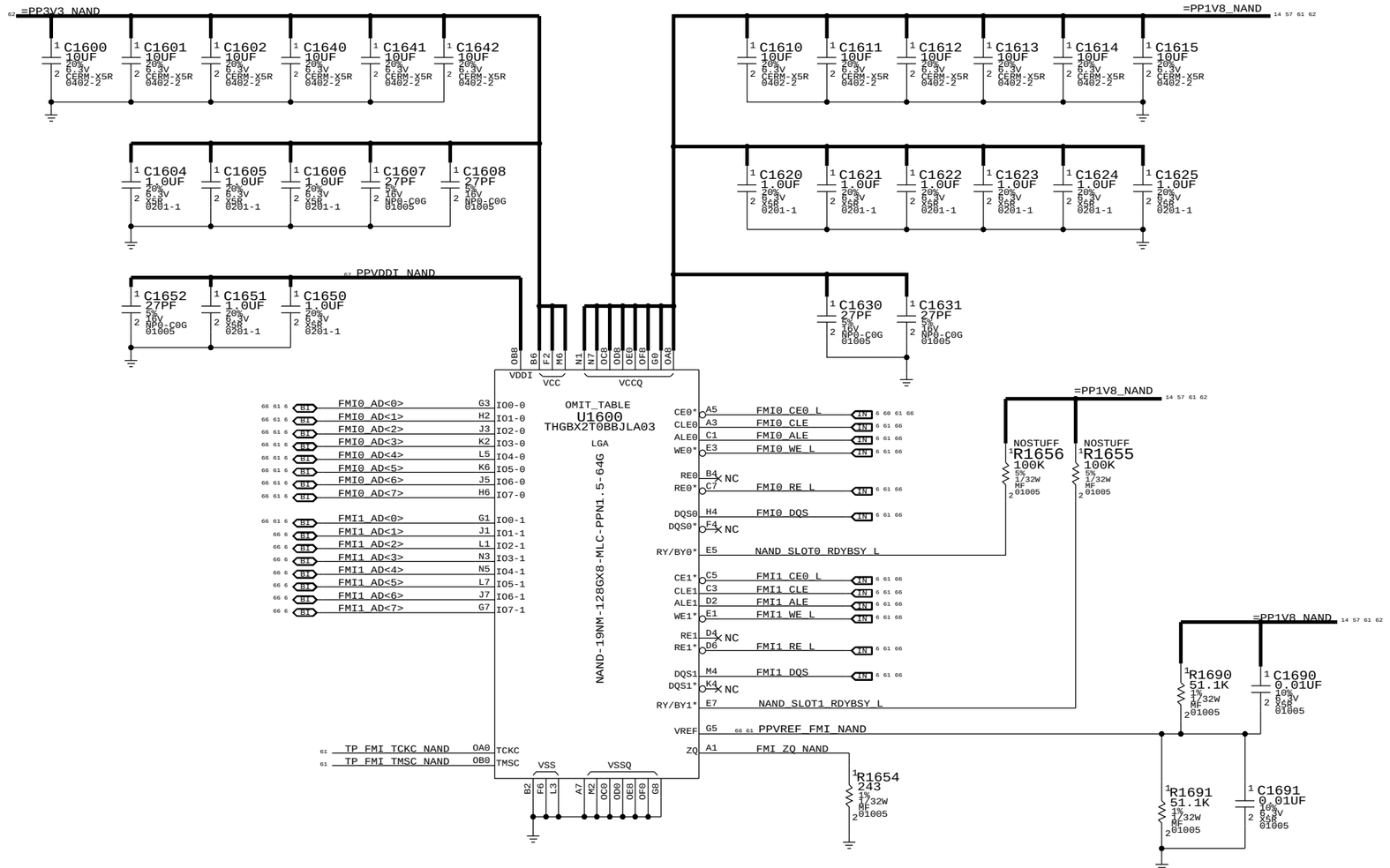
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ



SHORTING RESET TO TRST HERE SO THEY CAN BE SEPARATED ON DEV BOARD
NOTE: WHEN USING A0 SOC
STUFF R1535
NOSTUFF R1536
CHANGE R0620 TO 4.7K

ALIASED NETS TO ALLOW BREAKING ON DEV BOARD

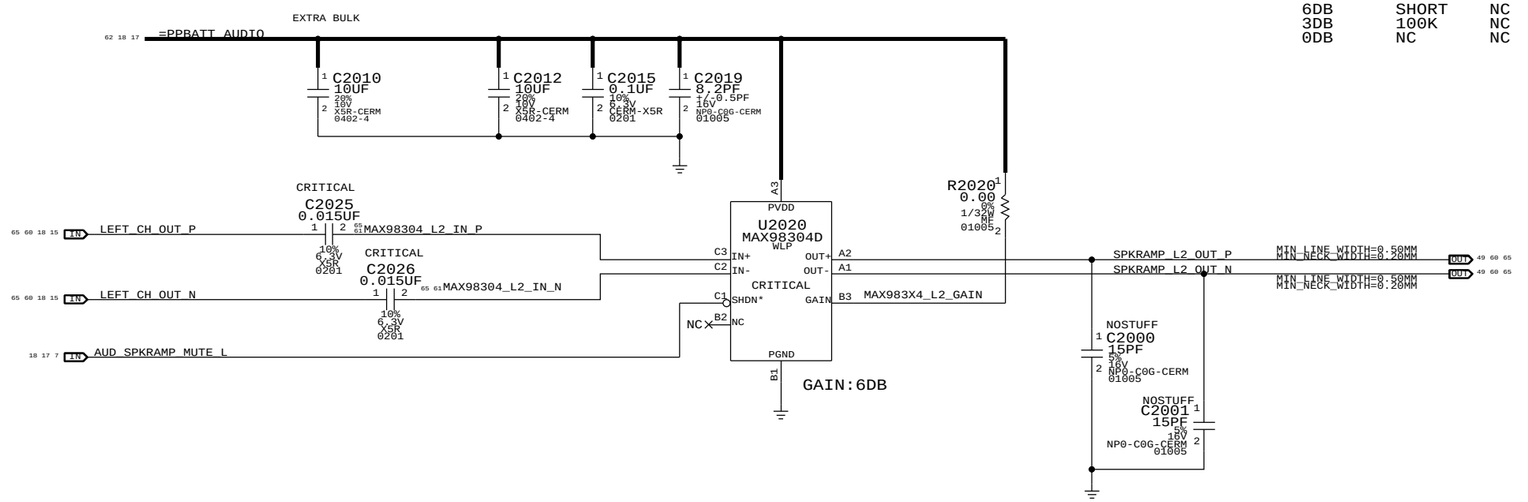


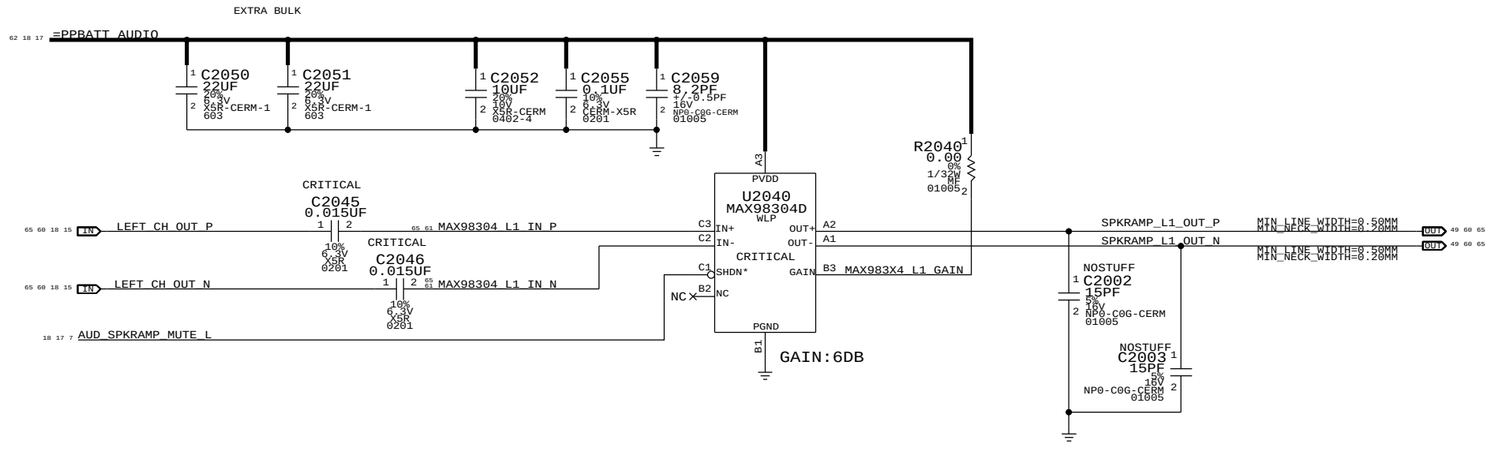


SPEAKER AMPLIFIER

APN:353S3445
TURN ON TIME: 3.5MS
75HZ +/- XXX% TURN ON DELAY: ?MS

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

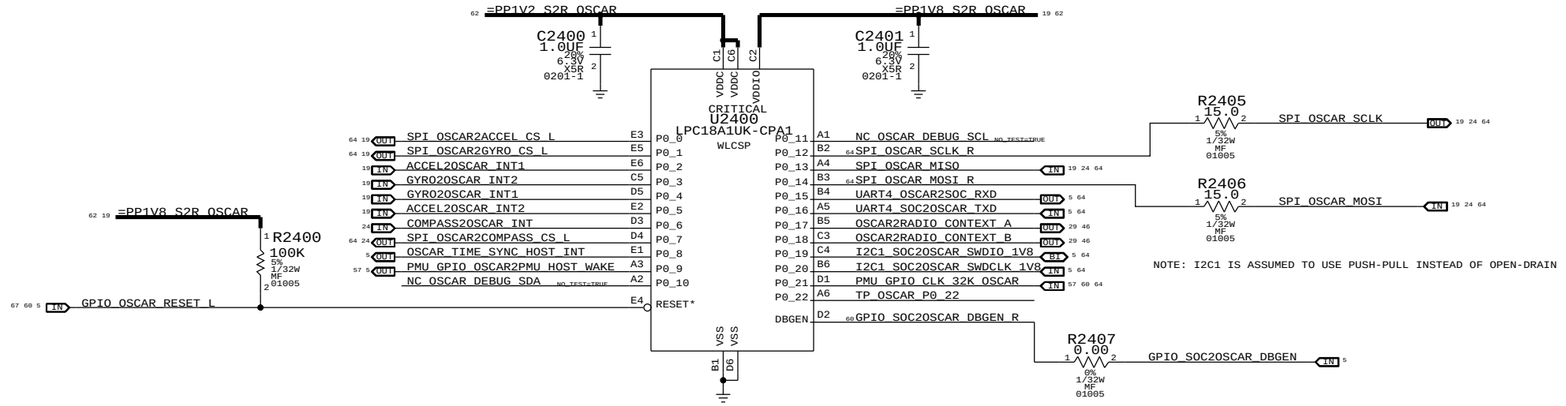




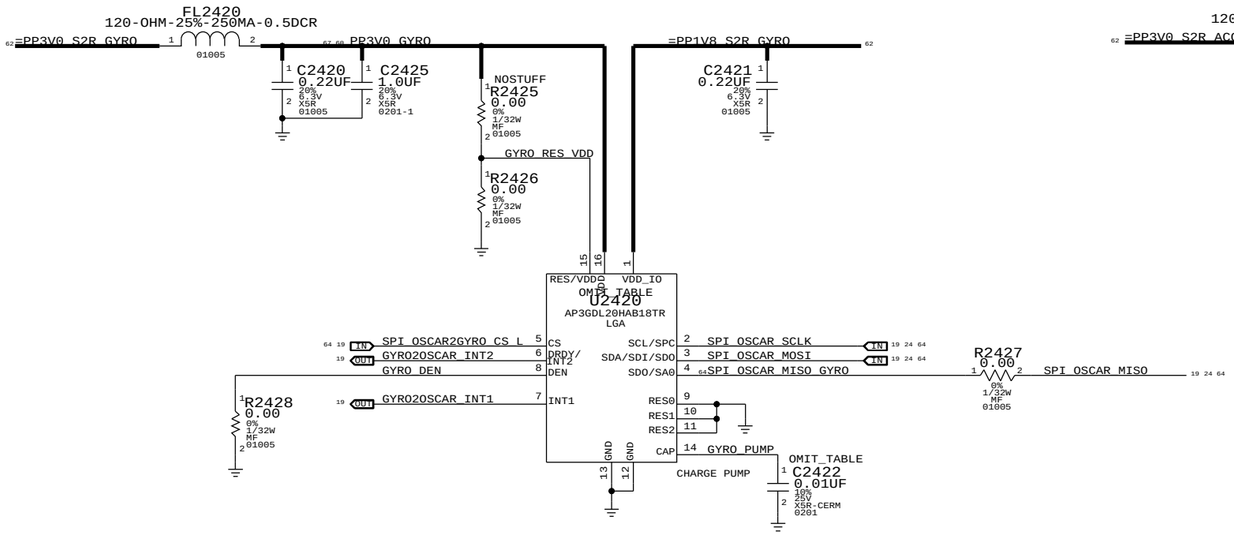
OSCAR

APN 337S4416 (A1)

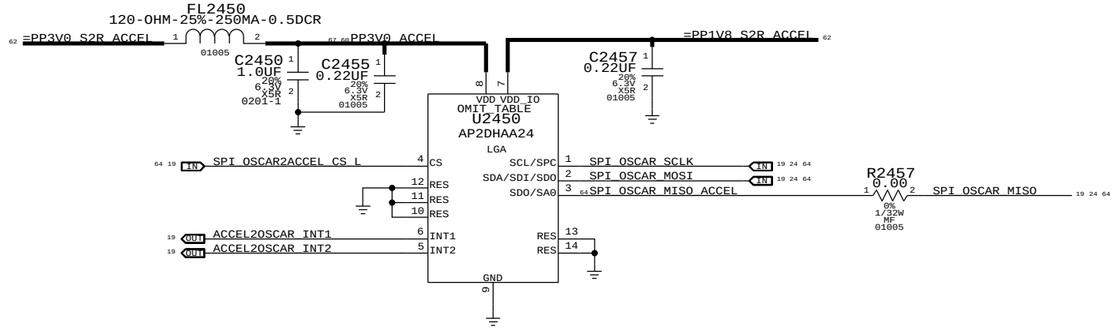
OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)



GYRO



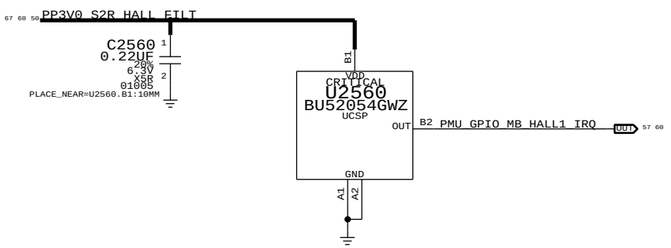
ACCELEROMETER



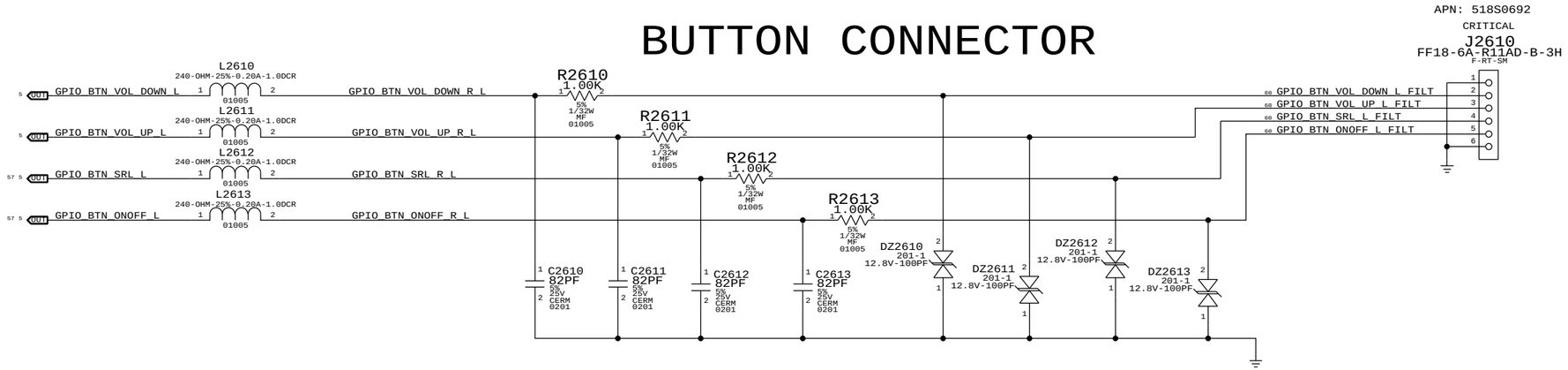
HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

C-PANEL HALL EFFECT SENSOR
(B-PANEL HALL EFFECT SENSOR ON HB)



BUTTON CONNECTOR

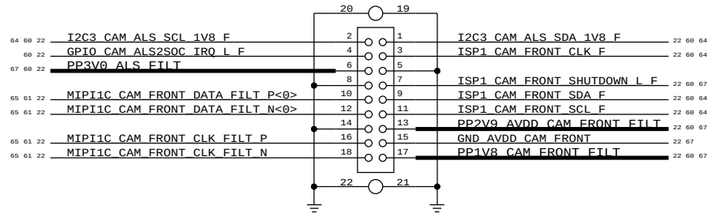


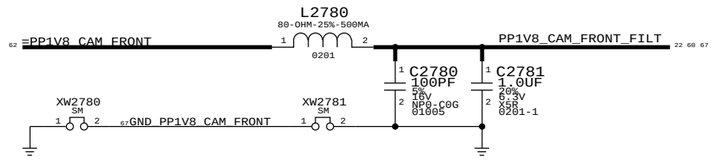
FRONT CAMERA CONNECTOR

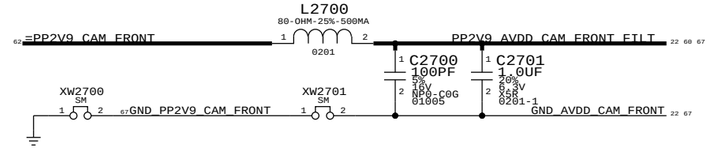
J65 CAMERA CONNECTOR

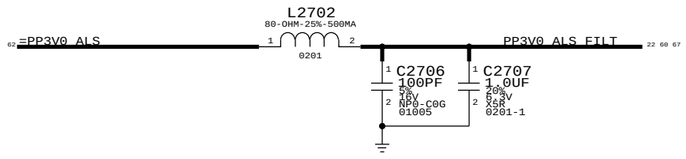
APN:MLB 516S0876
APN:FLEX 516S0869

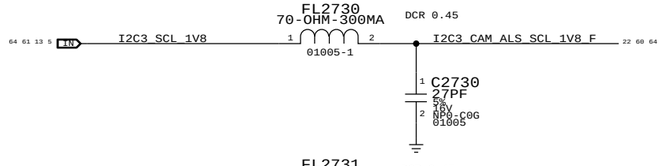
CRITICAL
J2700
503548-1820
F-ST-SM

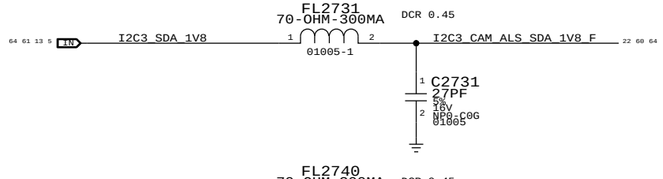


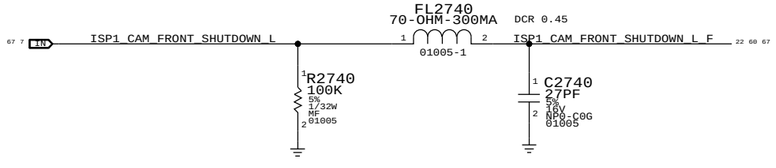


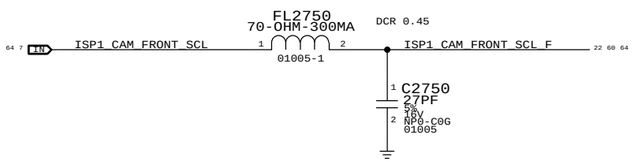


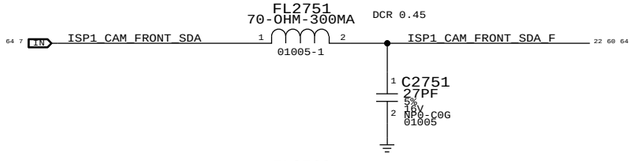


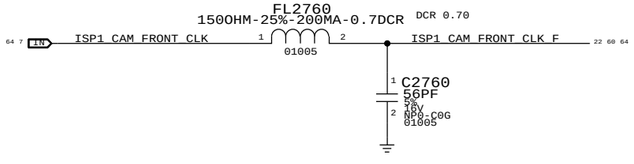


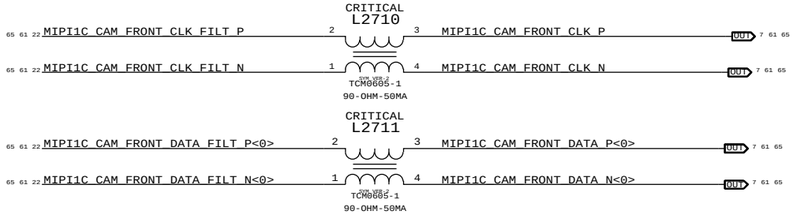






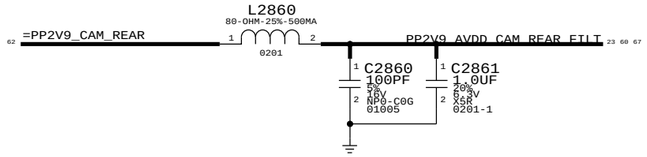


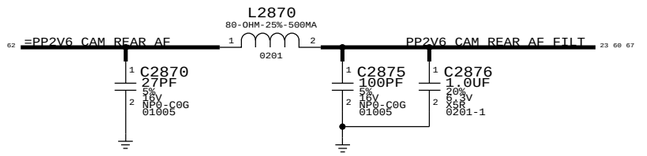


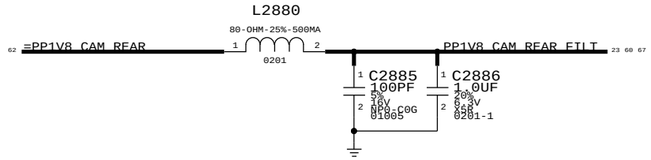


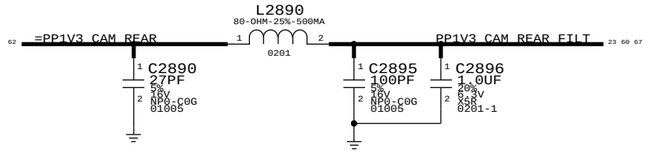
REAR CAMERA CONNECTOR

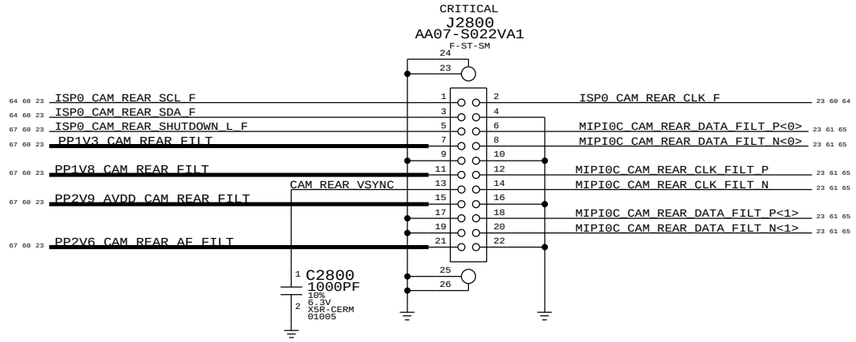
FLEX: 516S0974
MLB: 516S0973

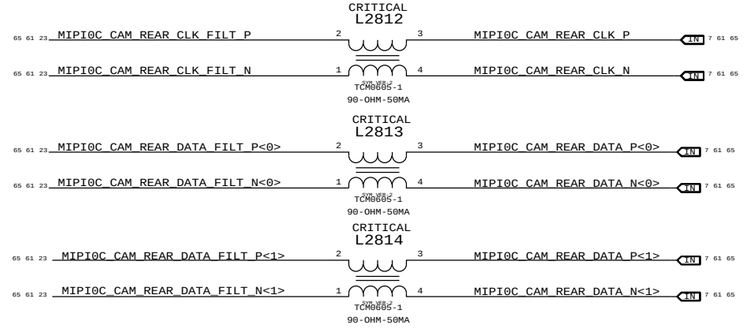


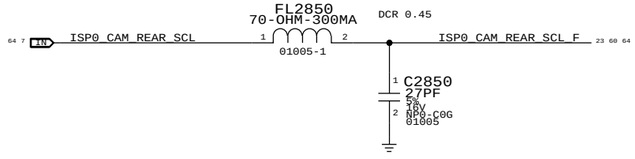


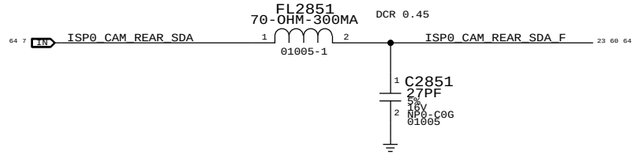


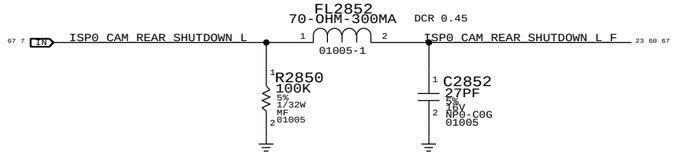


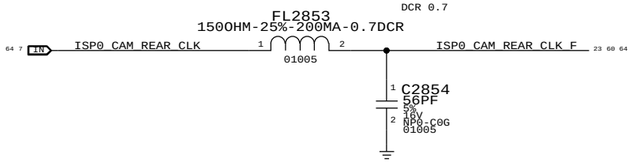






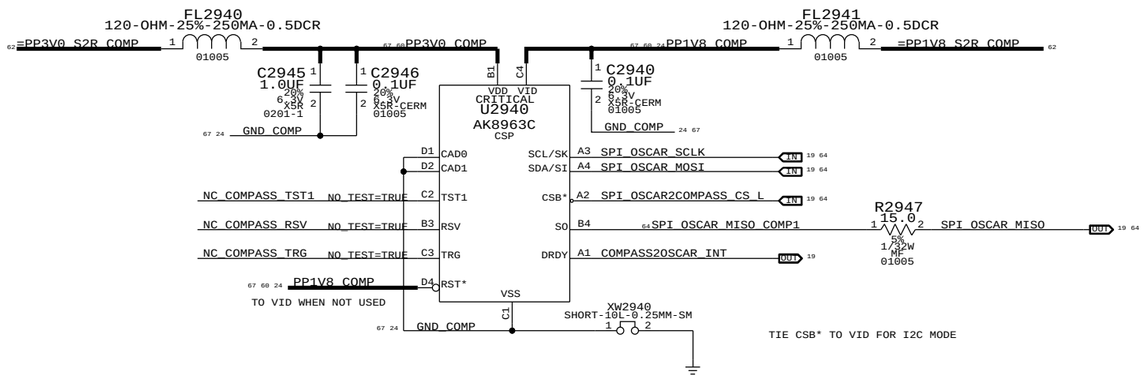






COMPASS

APN 338S1014



AP INTERFACE & DEBUG CONNECTOR

PROBE POINTS

PP3000 — P4MM SM — PP — 1 BB_ERROR_FLAG — 29 68
PP3001 — P4MM SM — PP — 1 SLEEP_CLK_32K — 27 28 68
PP3002 — P4MM SM — PP — 1 PMIC_SSBI — 27 28 68
PP3003 — P4MM SM — PP — 1 19P2M_MDM — 27 28 68
PP3008 — P4MM SM — PP — 1 WTR_SSBI_TX_GPS — 29 30
PP3009 — P4MM SM — PP — 1 WTR_SSBI_PRX_DRX — 29 30
PP3010 — P4MM SM — PP — 1 WTR_RX_ON — 29 30 68
PP3011 — P4MM SM — PP — 1 WTR_RF_ON — 29 30 68
PP3012 — P4MM SM — PP — 1 UART_WLAN2BB_LTE_COEX — 29 46
PP3013 — P4MM SM — PP — 1 UART_BB2WLAN_LTE_COEX — 29 46

DEBUG CONNECTOR

=PPBATT_VCC_BB — IN — 26 34 35 36 37 38 39 40 62

J3003
AXE654124
M-ST-SM
NOSTUFF

	56	55	
	2	1	
	4	3	
	6	5	
60 27 OUT PS_HOLD_PMIC	8	7	GPIO_SOC2BB_RST_L — OUT — 5 27 60 67
60 27 5 OUT GPIO_SOC2BB_RADIO_ON_L	10	9	PP_SMPS3_MSME_1V8 — IN — 25 26 28 29 31 60
67 60 57 27 OUT PMU_GPIO_PMU2BBPMU_RST_L	12	11	RESET_SOC_L — OUT — 4 13 47 57 60 61 67
68 28 27 IN PMIC_RESOUT_L	14	13	
	16	15	UART3_BB2SOC_TX — IN — 5 29 47 64
	18	17	GPIO_DEBUG_LED — IN — 29
	20	19	
	22	21	UART3_SOC2BB_TX — OUT — 5 29 47 64
67 61 28 OUT DEBUG_RST_L	24	23	UART3_BB2SOC_RTS_L — IN — 5 29 64
64 61 28 5 OUT BB_JTAG_TMS	26	25	UART3_SOC2BB_RTS_L — OUT — 5 29 64
64 61 28 5 OUT BB_JTAG_TRST_L	28	27	
64 61 28 5 OUT BB_JTAG_TCK	30	29	
64 61 28 5 IN BB_JTAG_TDO	32	31	
64 61 28 5 OUT BB_JTAG_TDI	34	33	PMU_GPIO_BB_VBUS_DET — OUT — 28 57 61 67
28 OUT BB_JTAG_RTCLK	36	35	
	38	37	
68 29 25 OUT LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6	40	39	
	42	41	
68 40 29 OUT 2G_FEM_S1 — GPIO54/BOOT_CONFIG_0	44	43	
60 57 29 IN PMU_GPIO_BB2PMU_HOST_WAKE	46	45	HSIC2_BB2SOC_DEVICE_RDY — IN — 5 29 64
68 40 29 25 OUT 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1	48	47	
29 OUT GPIO_51 — GPIO51/BOOT_CONFIG_3	50	49	GPIO_BB2SOC_RESET_DET_L — IN — 5 29 67
	52	51	HSIC2_SOC2BB_HOST_RDY — IN — 5 29 64
	54	53	
	58	57	

XW3002 — SHORT-10L-0.25MM-SM
64 47 BI USB_BB_N
64 61 28 BI USB_BB_DEBUG_N
64 61 28 BI USB_BB_DEBUG_P

XW3003 — SHORT-10L-0.25MM-SM
64 47 BI USB_BB_P

PP_SMPS3_MSME_1V8 — 25 26 28 29 31 60

NOSTUFF R3002 10K 5% 1/32W MF 01005
NOSTUFF R3003 10K 5% 1/32W MF 01005

68 29 25 LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6
68 40 29 25 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1

BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION 6 (47)	5 (48)	4 (49)	3 (50)	2 (51)	1 (52)	0 (53)	(54)	(55)
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	1	0	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	1	0	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	1	1	0	X
ENABLE SAHARA PROTOCOL	0X08	X	1	0	0	1	0	X	X	X

J3002
MM4829-2702
F-ST-SM
NOSTUFF
1 HSIC2_BB_DATA — 4 28 61 64
2 3 4

J3001
MM4829-2702
F-ST-SM
NOSTUFF
1 HSIC2_BB_STB — 4 28 61 64
2 3 4

BASEBAND PMU (1 OF 2)

U3300
PM8018-0
BGA
VREG
(SYM 5 OF 5)
CRITICAL

=PPBATT_VCC_BB
C3200 10UF 20% 6.3V CERM-X5R 0402-2
C3201 10UF 20% 6.3V CERM-X5R 0402-2
C3202 10UF 20% 6.3V CERM-X5R 0402-2
C3203 56PF 5% 16V NP0-C0G 01005

XW3200 SHORT-10L-0.1MM-SM
REF_BYP
C3209 0.1UF 20% 6.3V X5R-CERM 01005
REF_GND

VDD_S1
VDD_S2
VDD_S3
VDD_S4
VDD_S5
C3204 4.7UF 20% 10V X5R-CERM 0402
C3205 4.7UF 20% 10V X5R-CERM 0402
C3206 4.7UF 20% 10V X5R-CERM 0402
C3207 4.7UF 20% 10V X5R-CERM 0402
C3208 4.7UF 20% 10V X5R-CERM 0402
S1_GND S2_GND S3_GND S4_GND S5_GND
VDD_XO
VDD_L2_L3
VDD_L4
VDD_L5_L6_L13_L14
PP_SMPS4_RF2_2V05
PP_SMPS3_MSME_1V8
PP_SMPS5_DSP_1V05
VDD_L7
VDD_L8
VDD_L9
VDD_L10_L11
VDD_L12

VOUT_LVS1
VREG_RFCLK
VSW_S1 VREG_S1
VSW_S2 VREG_S2
VSW_S3
VSW_S5_2 VREG_S3
VSW_S4 VREG_S4
VSW_S5 VREG_S5
PP_VSW_S1
PP_VSW_S2
PP_VSW_S3
PP_VSW_S4
PP_VSW_S5
VREG_XO VREG_L2 VREG_L3 VREG_L4 VREG_L5 VREG_L6 VREG_L13 VREG_L14 VREG_L7 VREG_L8 VREG_L9 VREG_L10 VREG_L11 VREG_L12

PP_LVS1
PP_VREG (INTERNAL USE ONLY)
C3230 1.0UF 20% 6.3V X5R 0201-1

L3200 2.2UH-20%-1.2A-0.150HM 0806 CRITICAL
PP_SMPS1_MSMC_1V05
C3229 22UF 20% 6.3V X5R-CERM-1 603
S1_GND

L3201 2.2UH-20%-1.2A-0.150HM 0806 CRITICAL
PP_SMPS2_RF1_1V3
C3228 22UF 20% 6.3V X5R-CERM-1 603
S2_GND

L3202 2.2UH-20%-1.2A-0.150HM 0806 CRITICAL
PP_SMPS3_MSME_1V8
C3226 22UF 20% 6.3V X5R-CERM-1 603
C3227 0.1UF 20% 10V X5R 0100S NOSTUFF
S3_GND

L3203 2.2UH-20%-1.2A-0.150HM 0806 CRITICAL
PP_SMPS4_RF2_2V05
C3225 22UF 20% 6.3V X5R-CERM-1 603
S4_GND

L3204 2.2UH-20%-2.34A-0.113OHM 2520-SM CRITICAL
PP_SMPS5_DSP_1V05
C3224 22UF 20% 6.3V X5R-CERM-1 603
S5_GND

PP_LDO1 (INTERNAL USE ONLY)
PP_LDO2_XO_HS_1V8
PP_LDO3_AMUX_1V8
PP_LDO4_VDDA_3V3
PP_LDO5_GPS_LNA_2V5
PP_LDO6_RUIM_1V8
PP_LDO13_VDDPX_2V95
PP_LDO14_2V65
PP_LDO7_DAC_1V8
PP_LDO8_VDDPX_1V2
PP_LDO9_PLL_1V05
PP_LDO10_ADSP_1V05
PP_LDO11_MDSP_FW_1V05
PP_LDO12_MDSP_SW_1V05

C3210 1.0UF 20% 6.3V X5R 0201-1
C3211 1.0UF 20% 6.3V X5R 0201-1
C3212 1.0UF 20% 6.3V X5R 0201-1
C3213 1.0UF 20% 6.3V X5R 0201-1
C3214 1.0UF 20% 6.3V X5R 0201-1
C3215 1.0UF 20% 6.3V X5R 0201-1
C3216 1.0UF 20% 6.3V X5R 0201-1
C3217 1.0UF 20% 6.3V X5R 0201-1
C3218 10UF 20% 6.3V CERM-X5R 0402-2
C3219 1.0UF 20% 6.3V X5R 0201-1
C3220 10UF 20% 6.3V CERM-X5R 0402-2
C3221 10UF 20% 6.3V CERM-X5R 0402-2
C3222 10UF 20% 6.3V CERM-X5R 0402-2
C3223 10UF 20% 6.3V CERM-X5R 0402-2
C3231 1.0UF 20% 6.3V X5R 0201-1

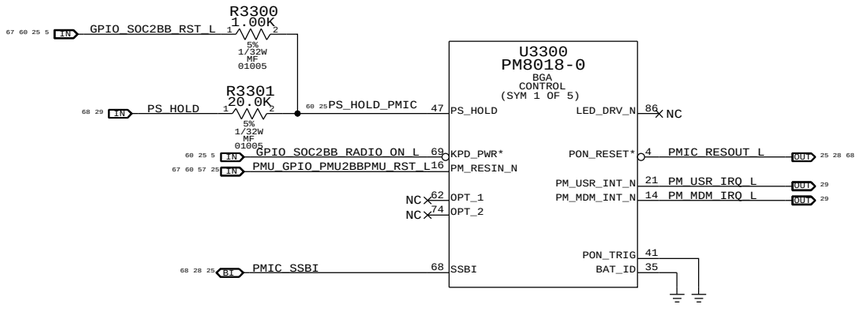
BASEBAND PMU (2 OF 2)

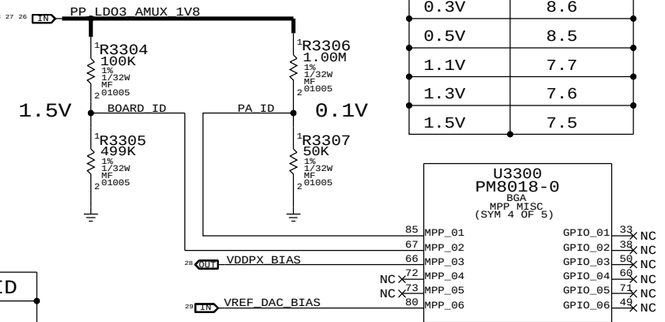
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

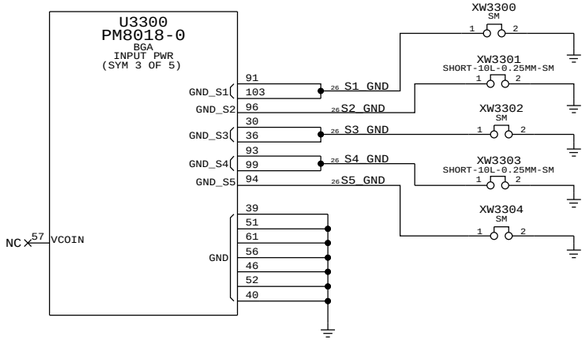
BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

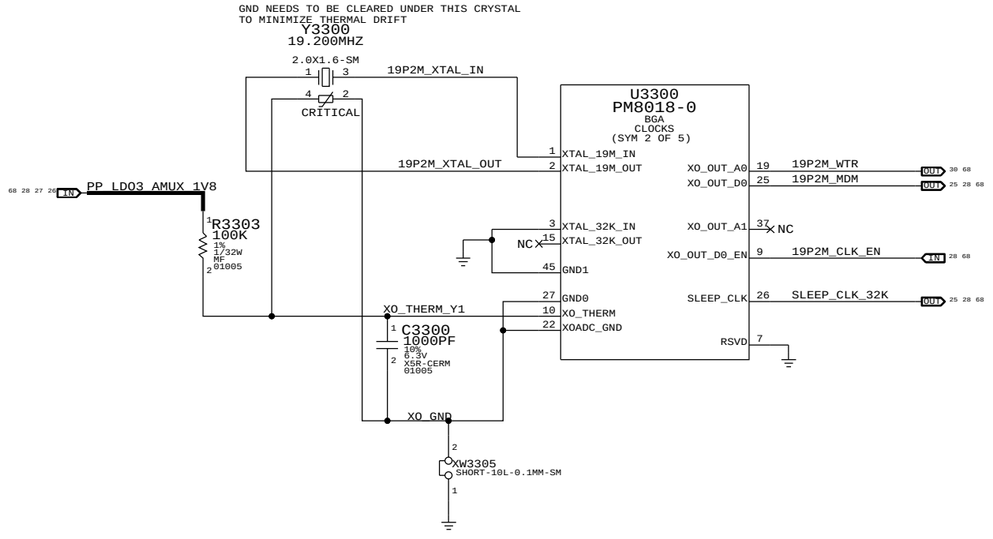
PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5





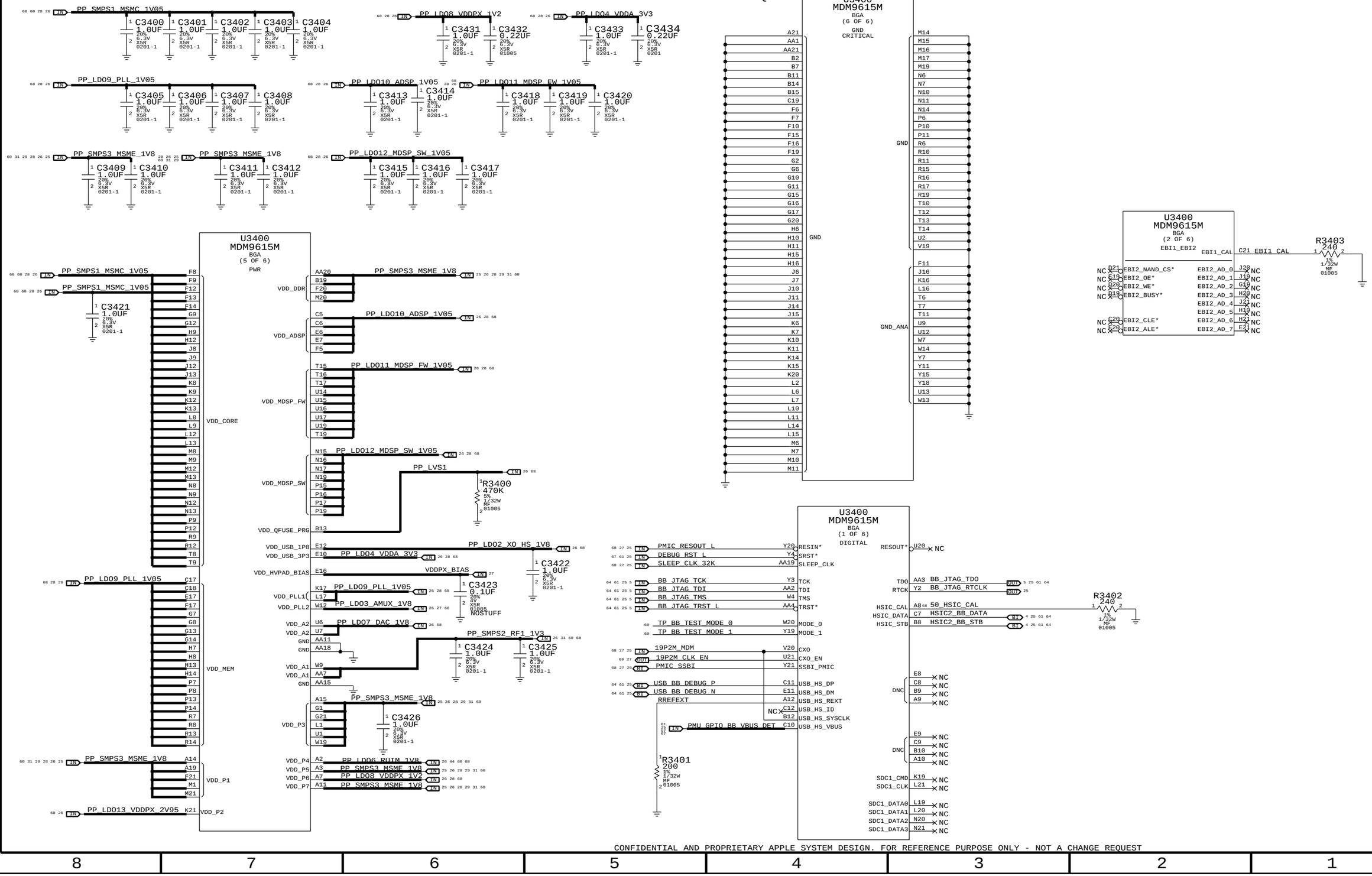
PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.





BASEBAND (1 OF 2)

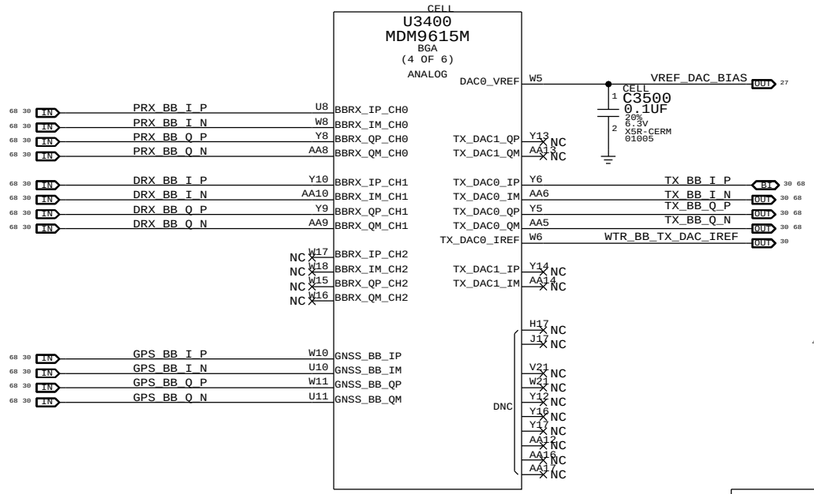
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST



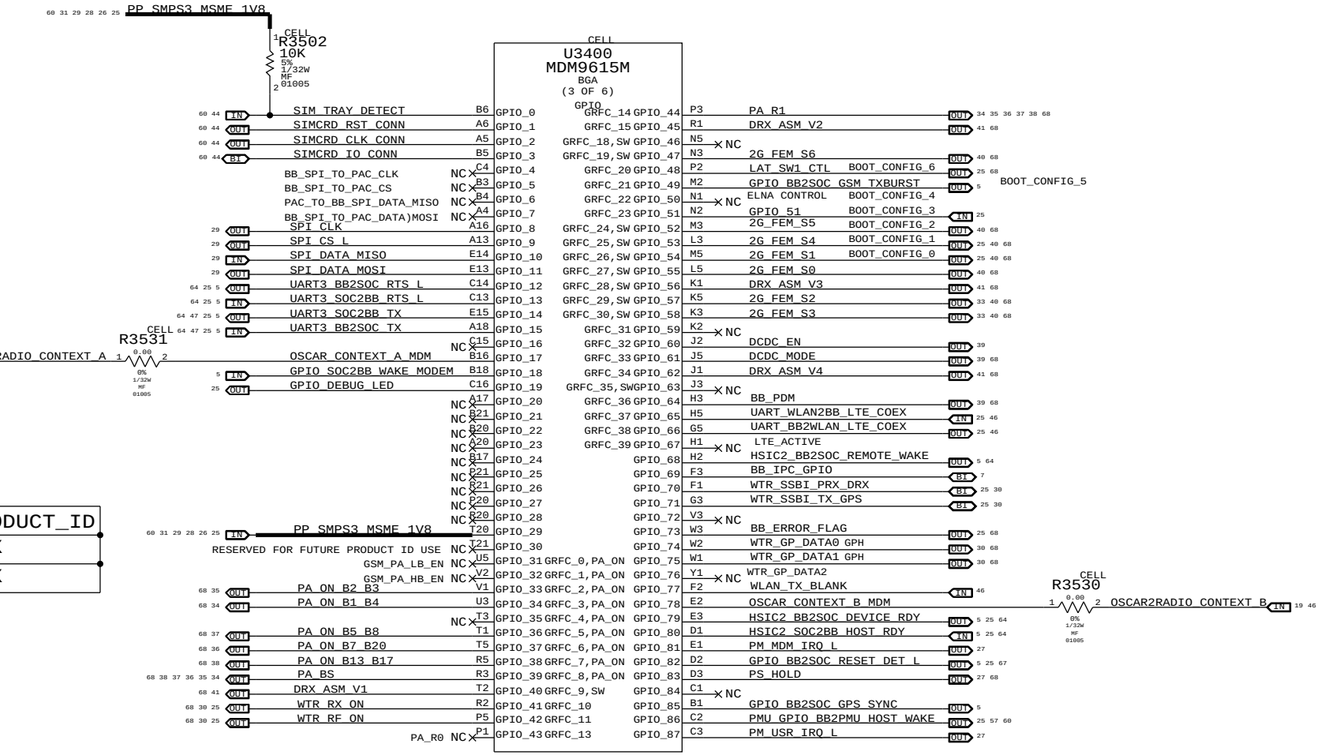
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSE ONLY - NOT A CHANGE REQUEST

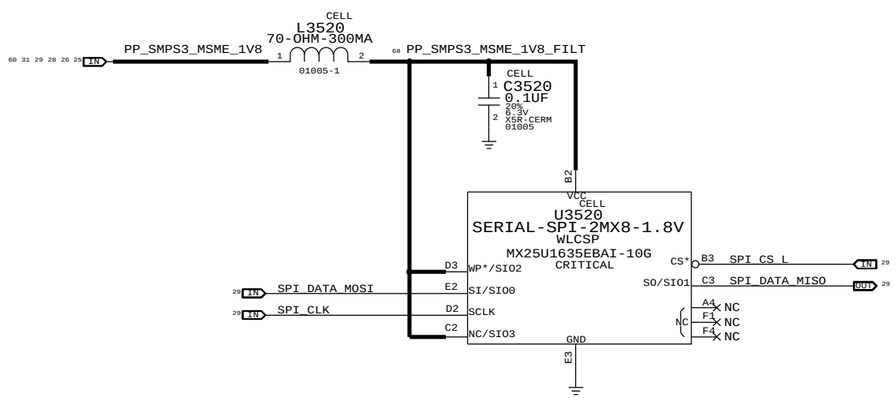
BASEBAND (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

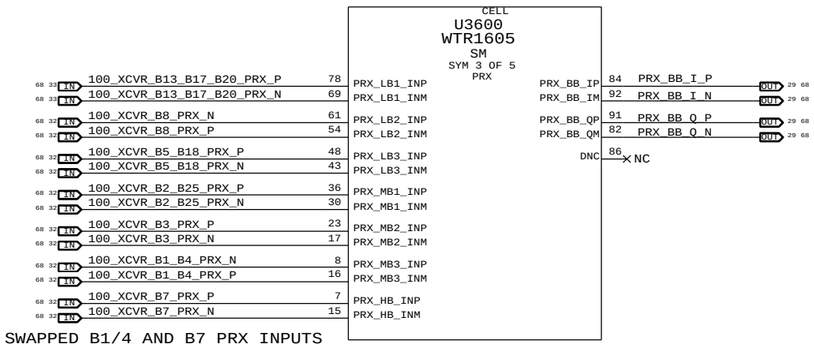




RF TRANSCEIVER (1 OF 2)

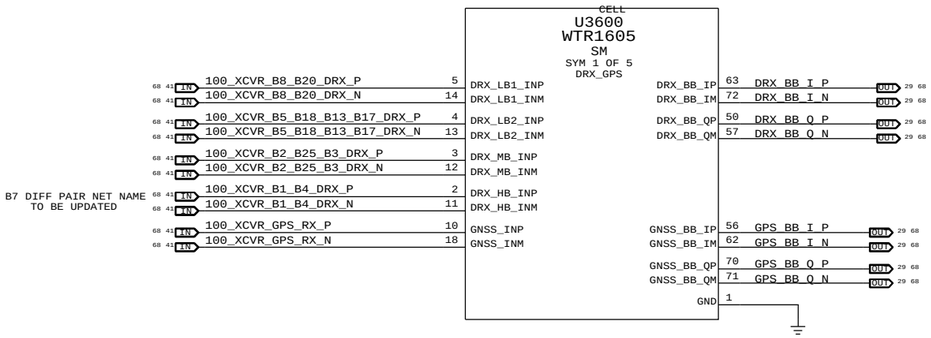
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

PRX TRANSCEIVER RF AND IQ PORTS



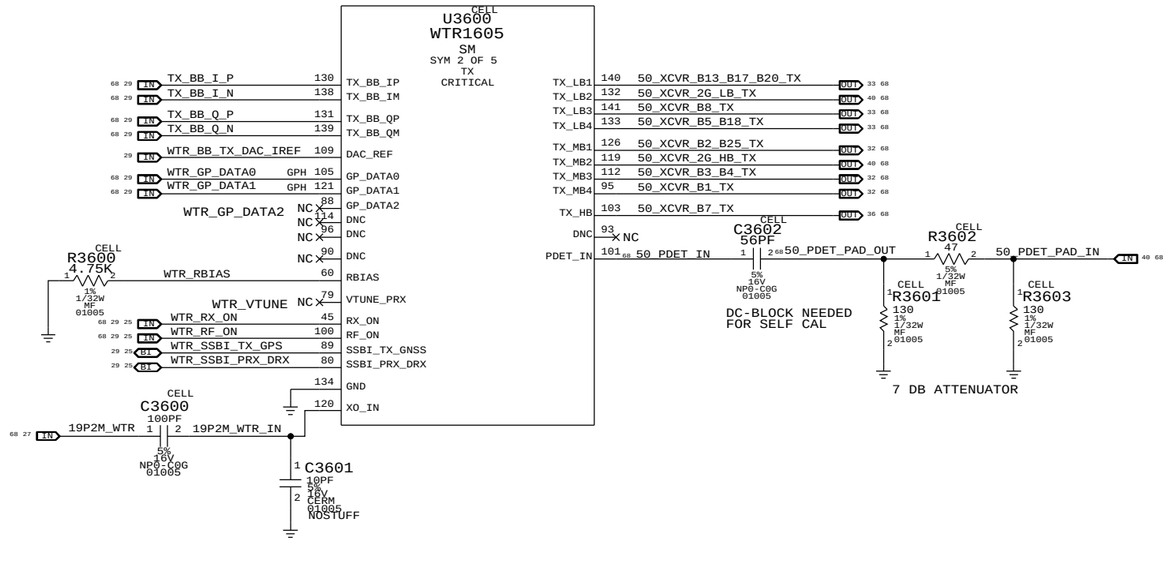
SWAPPED B1/4 AND B7 PRX INPUTS

DRX TRANSCEIVER RF AND IQ PORTS

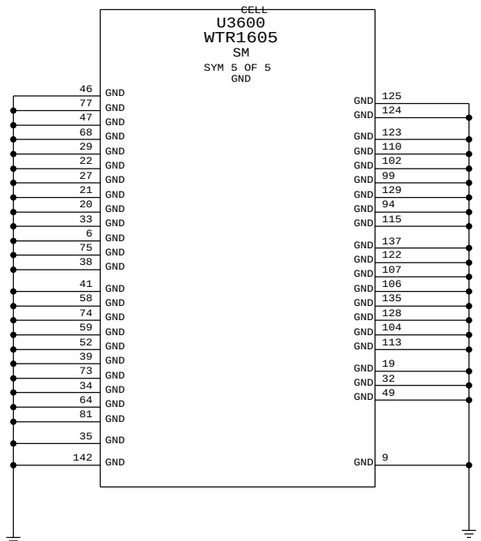


B7 DIFF PAIR NET NAME TO BE UPDATED

TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS

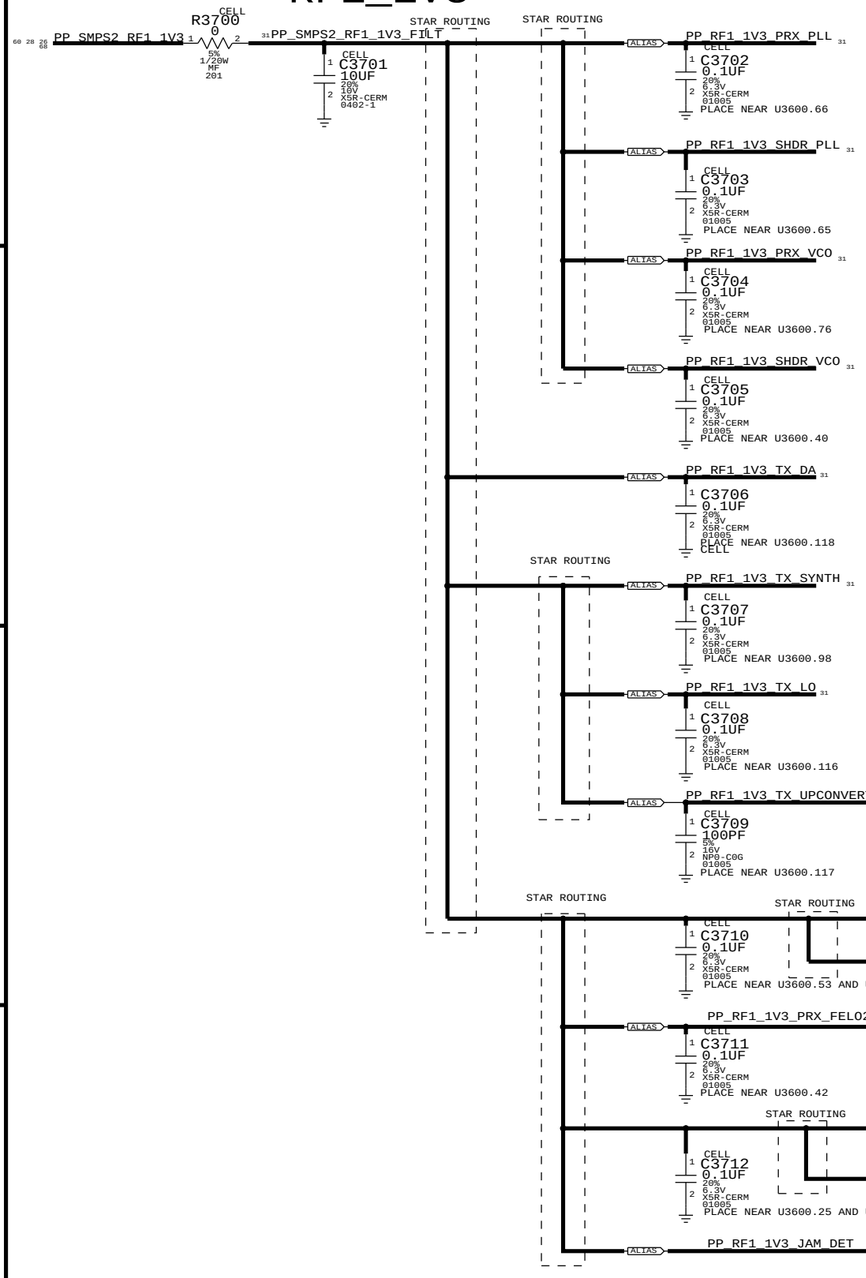


TRANSCEIVER GROUND CONNECTIONS

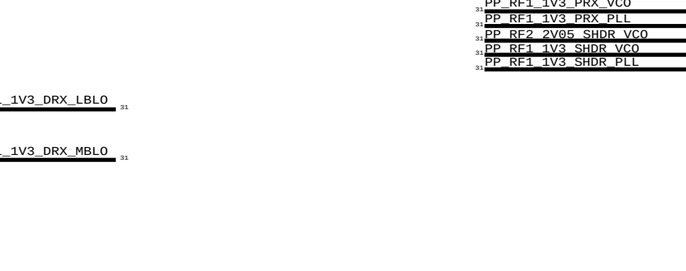


RF TRANSCEIVER (2 OF 2)

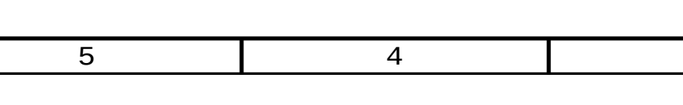
RF1_1V3



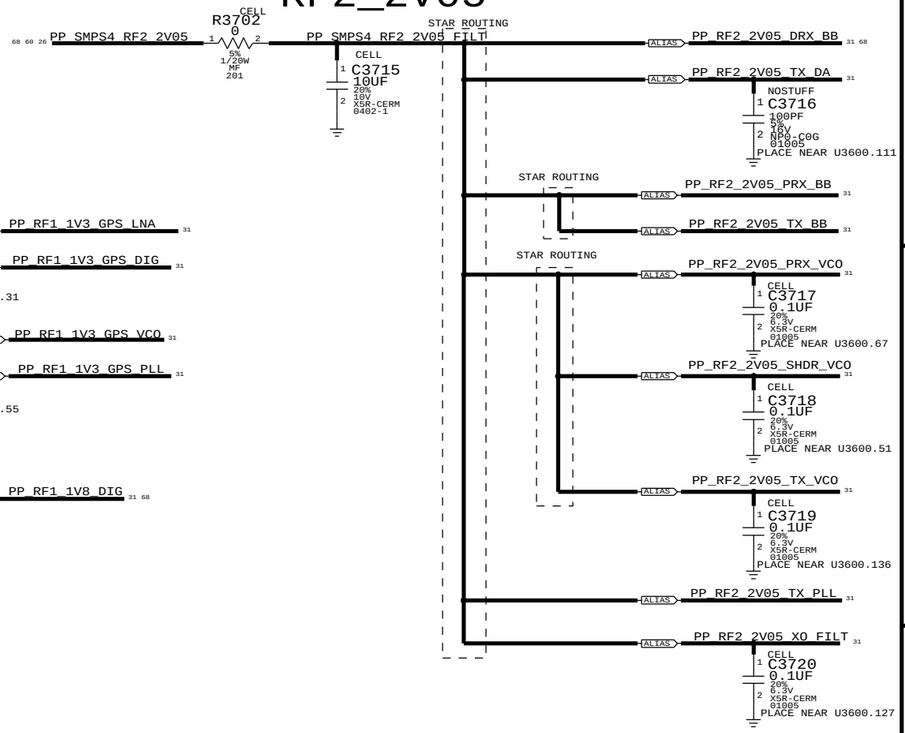
RF1_1V3



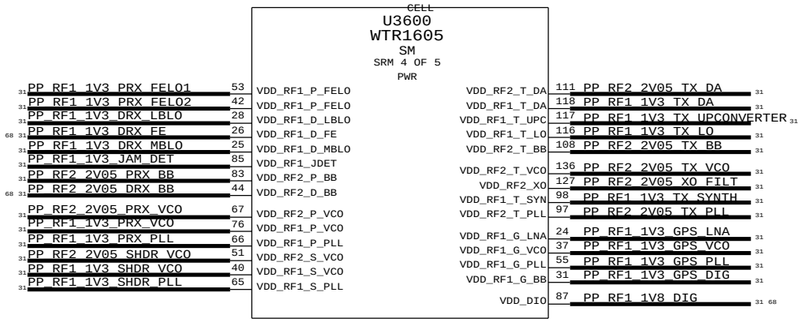
RF1_1V8



RF2_2V05

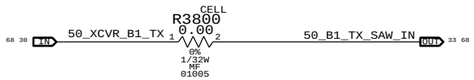


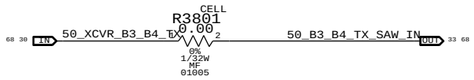
TRANSCEIVER POWER CONNECTIONS

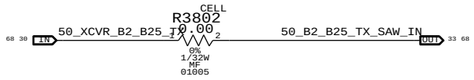


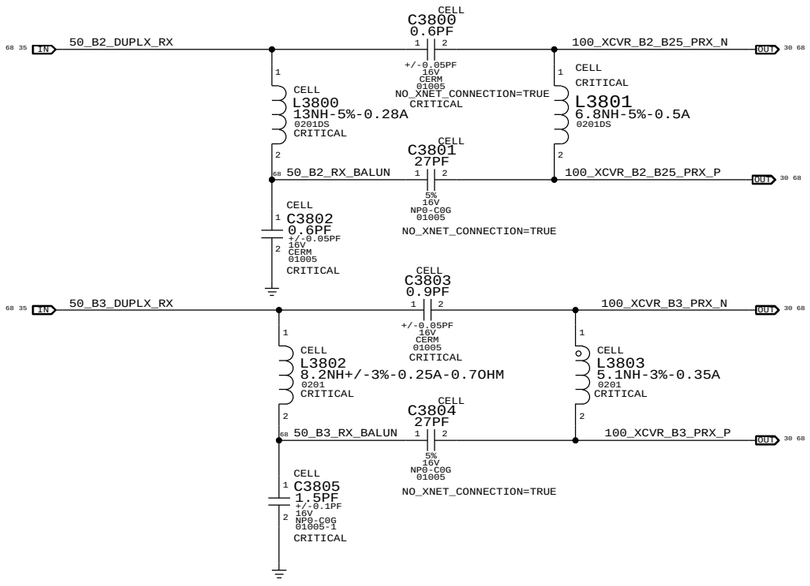
TRANSCEIVER TX AND RX MATCHING NETWORKS

TX MATCHING NETWORKS

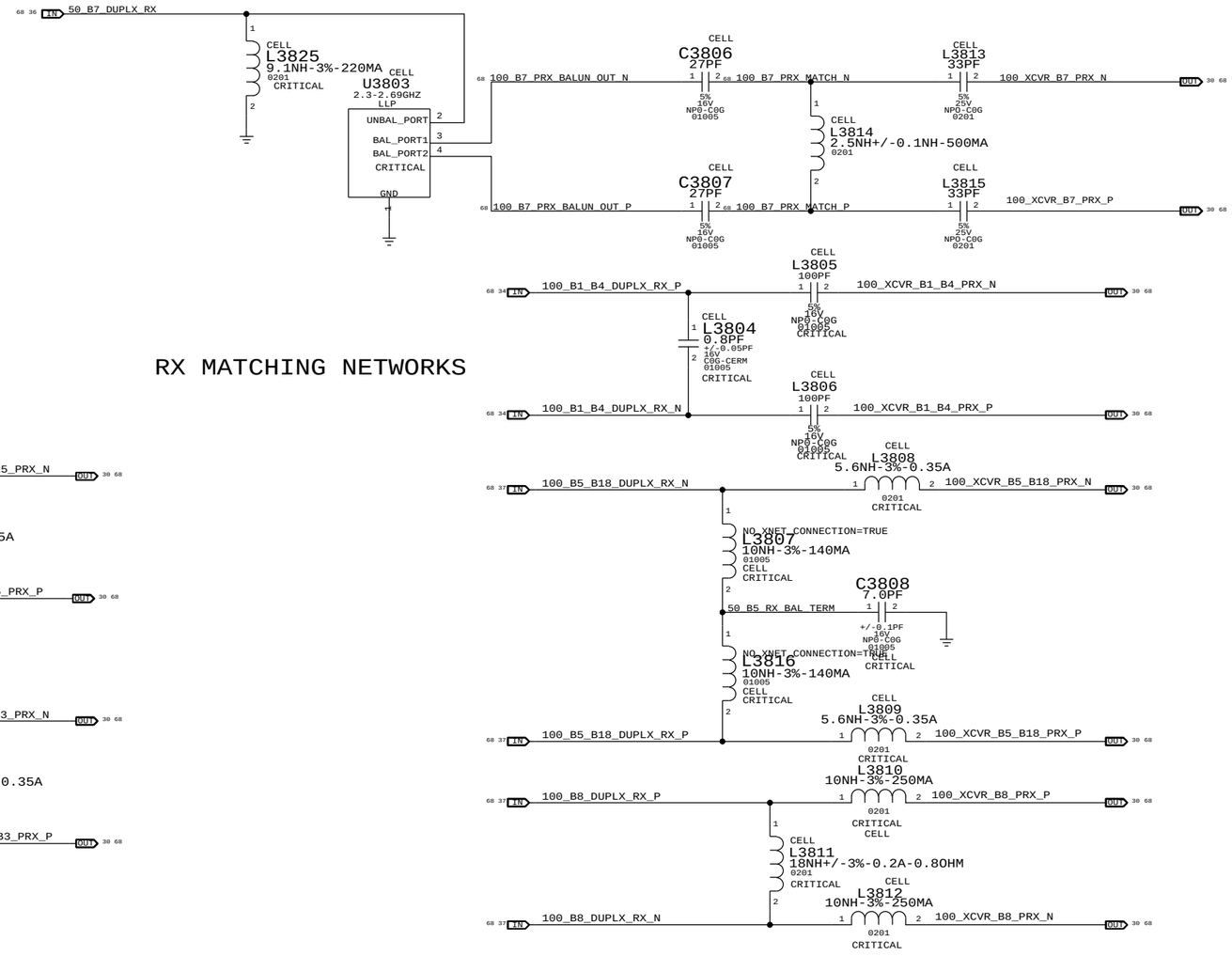








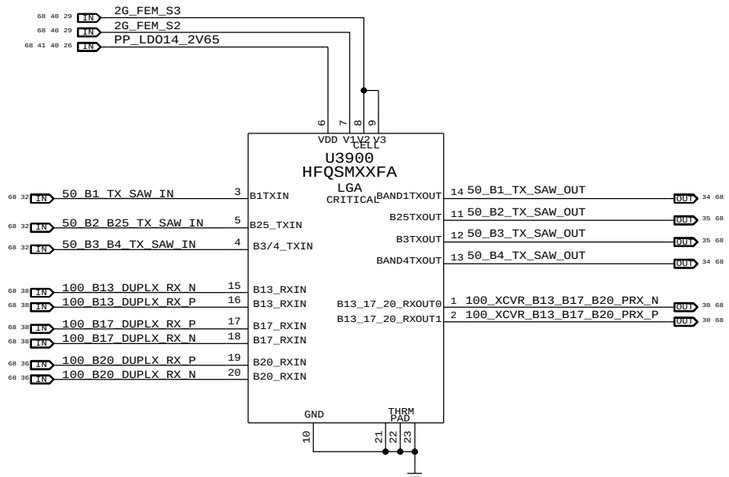
RX MATCHING NETWORKS



SAW BANK

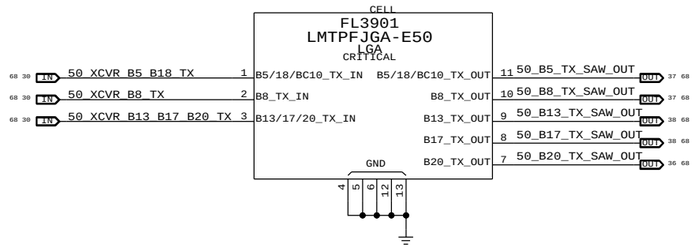
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

HB TX SAW BANK +
B13/B17/B20 DP6T SWITCH AND MATCHING



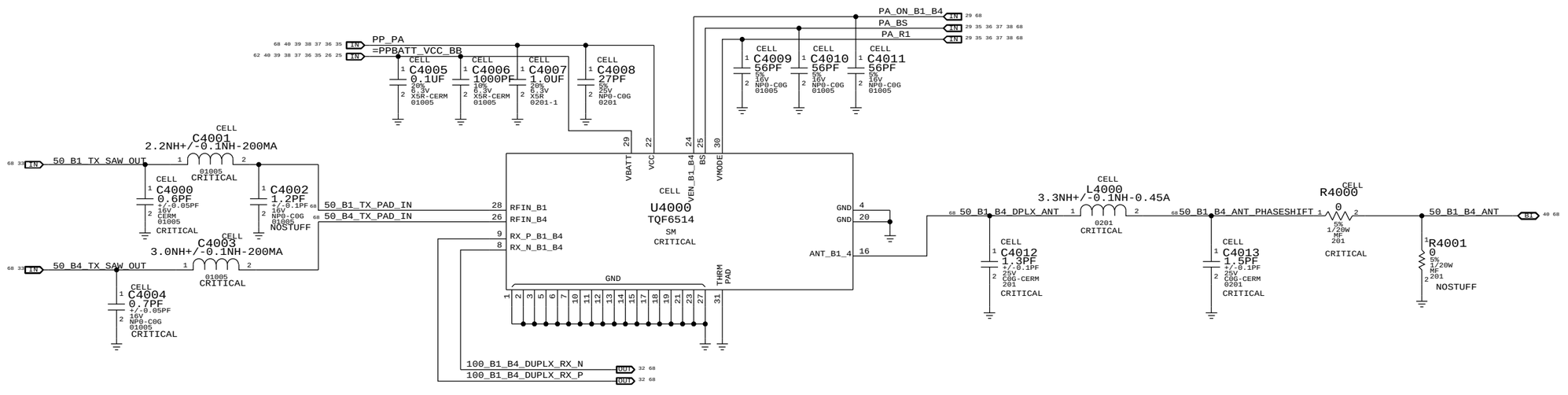
BAND	V3=V2	V1
B3 TX	HIGH	X
B4 TX	LOW	X
B13 RX	HIGH	HIGH
B17 RX	HIGH	LOW
B20 RX	LOW	HIGH

LB TX SAW BANK



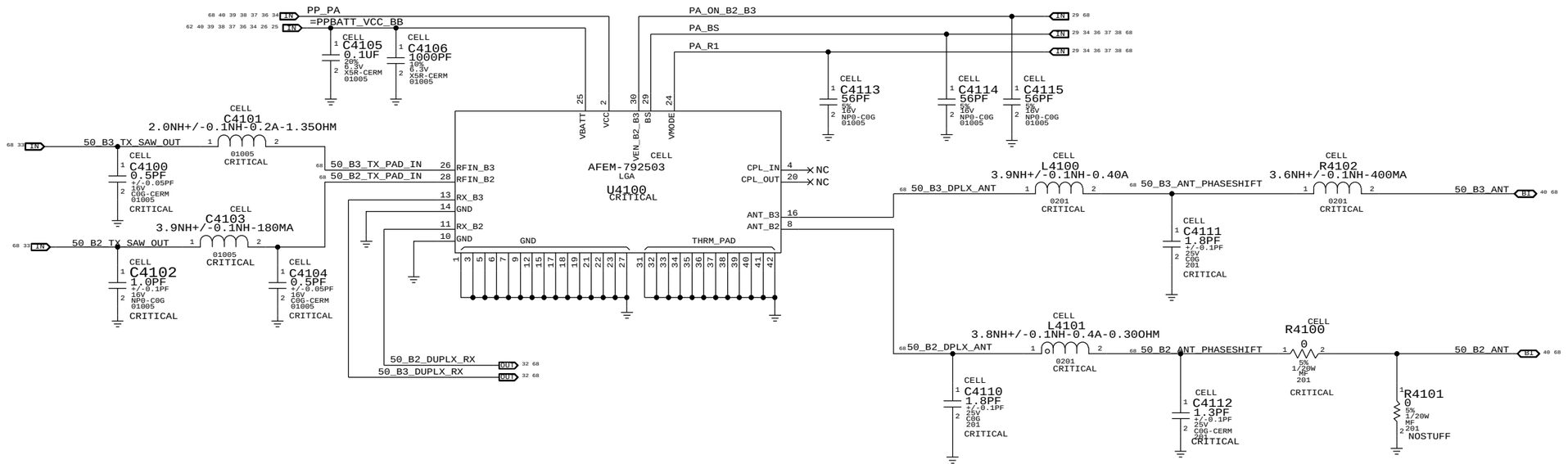
BAND 1/4 PAD

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B1_B4	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B4	HPM	0	1	0
B4	LPM	0	1	1
B1	HPM	1	1	0
B1	LPM	1	1	1

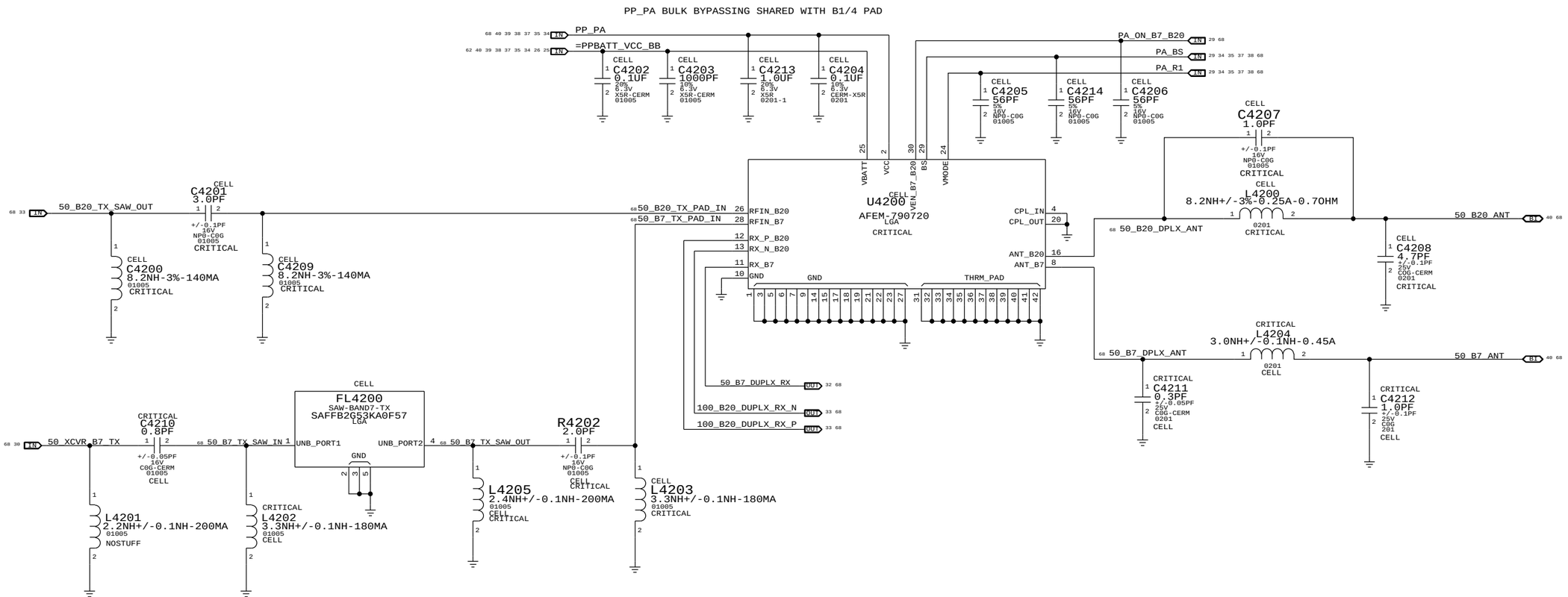
BAND 2/3 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

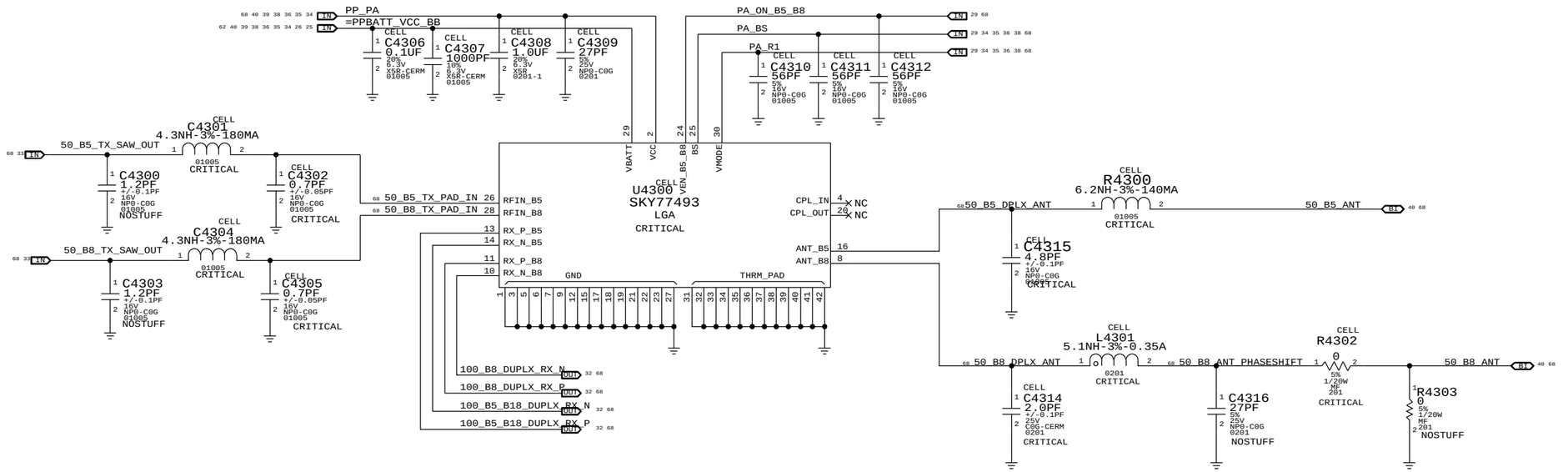
BAND 20/7 PAD

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



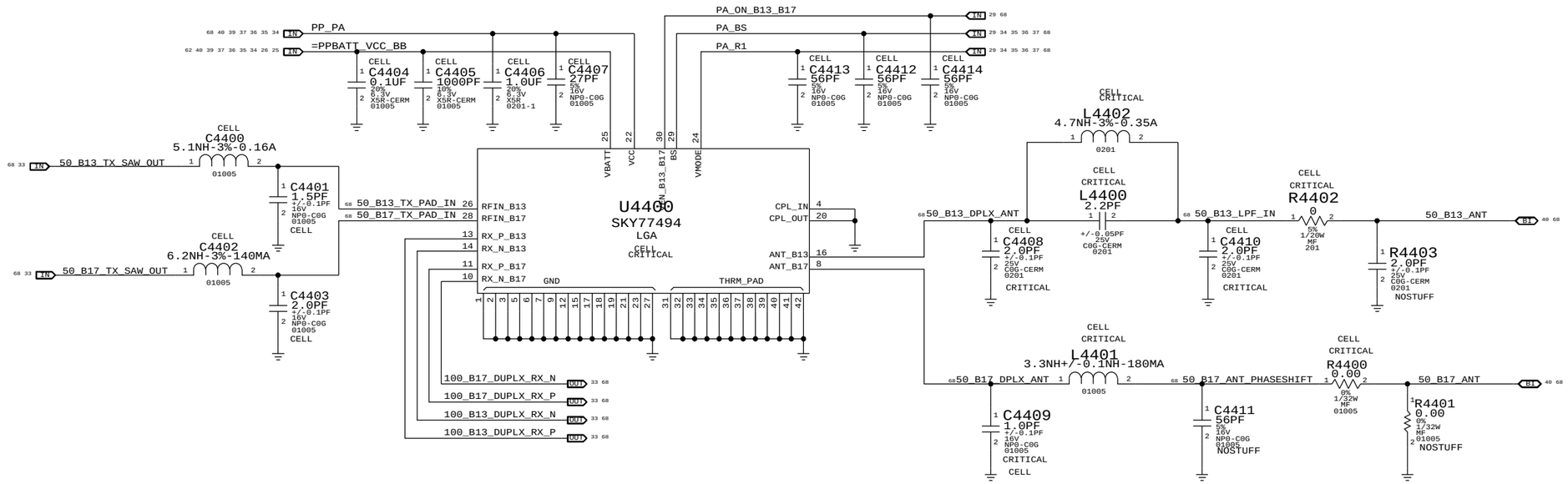
BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

BAND 5/8 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

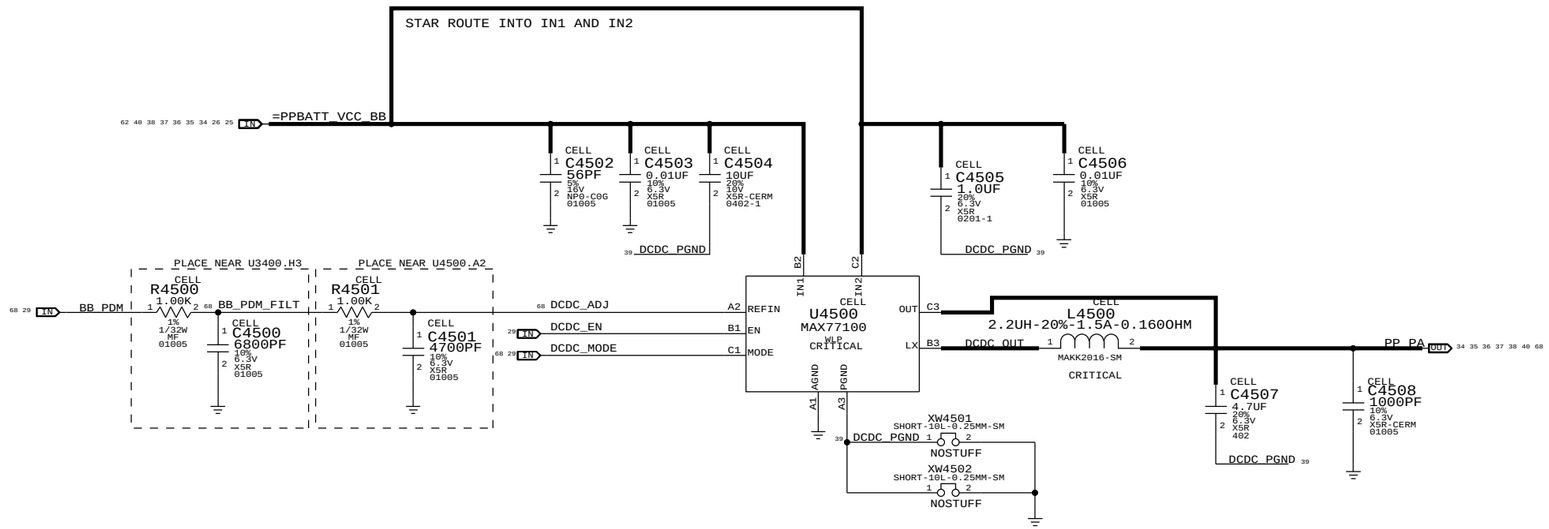
BAND 13/17 PAD



BAND	PA_POWER_MODE	PA_BS	PA_ON_B13_B17	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

PA DC/DC CONVERTER

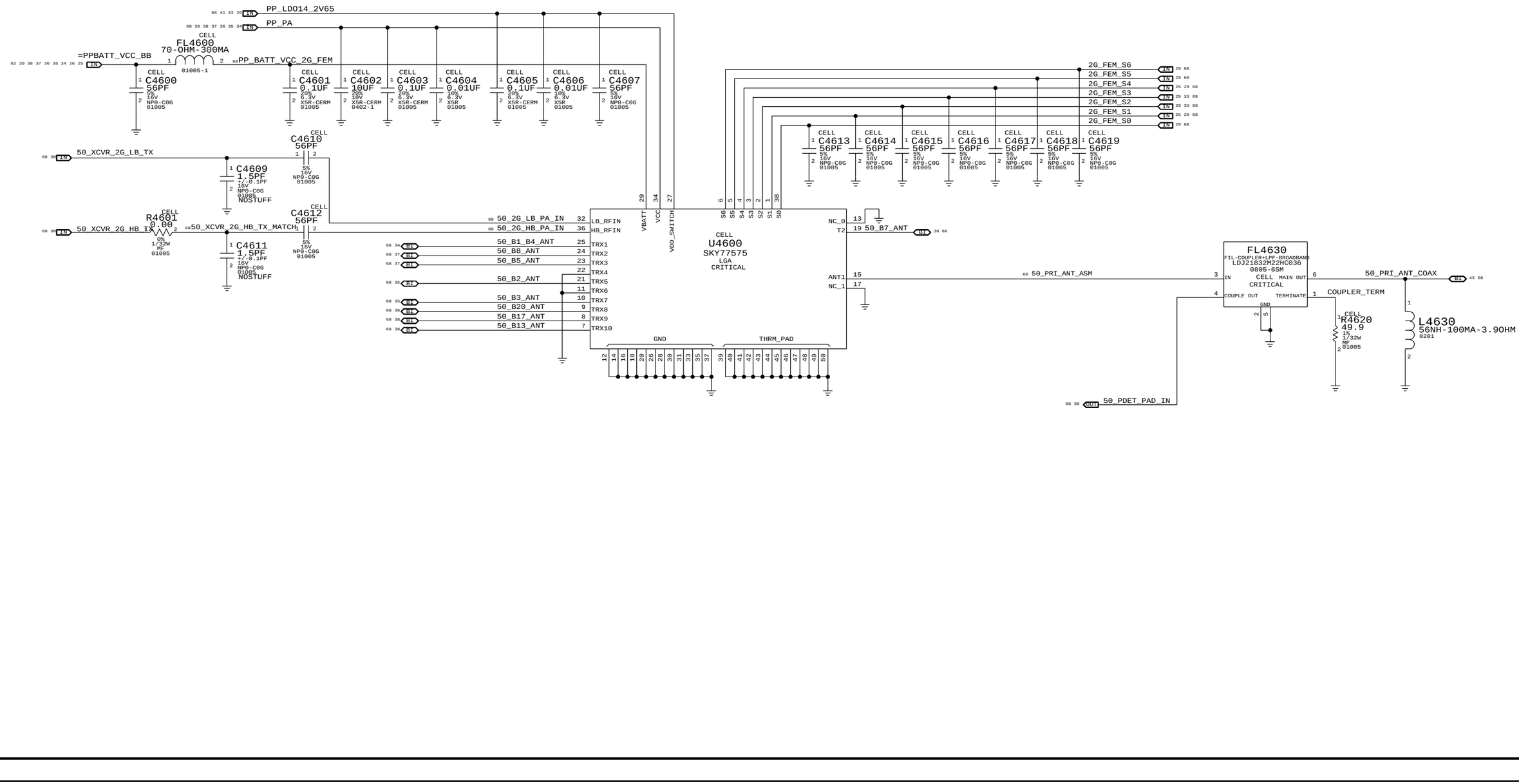
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



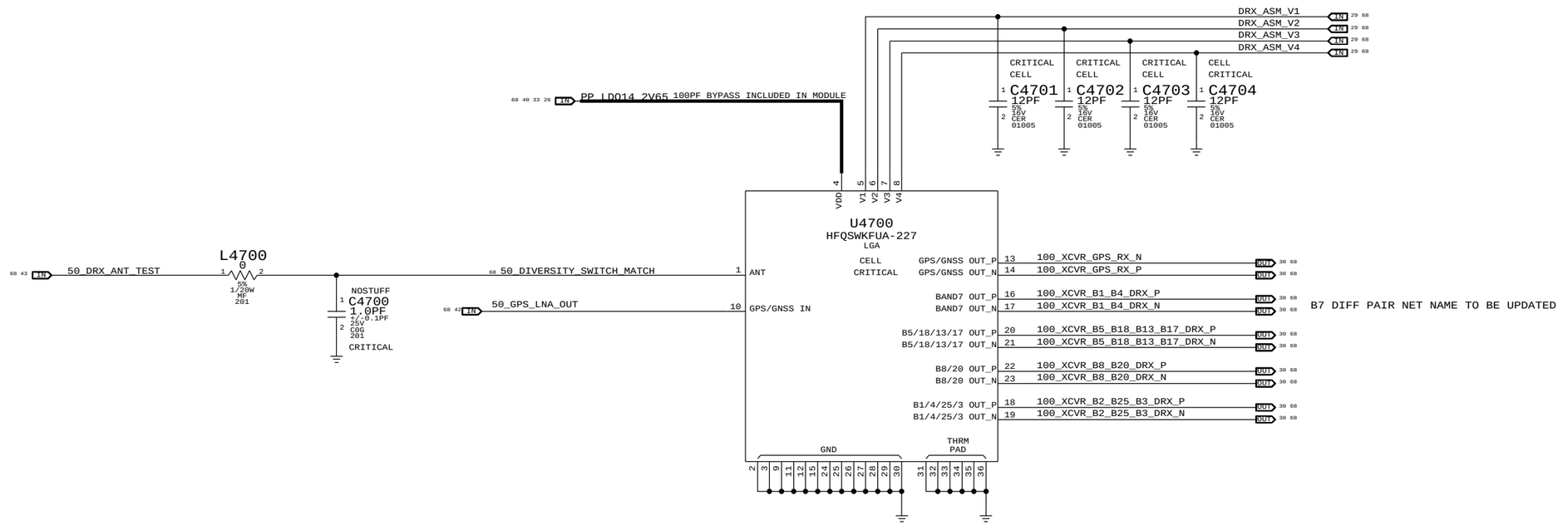
2G FEM

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

2G FEM



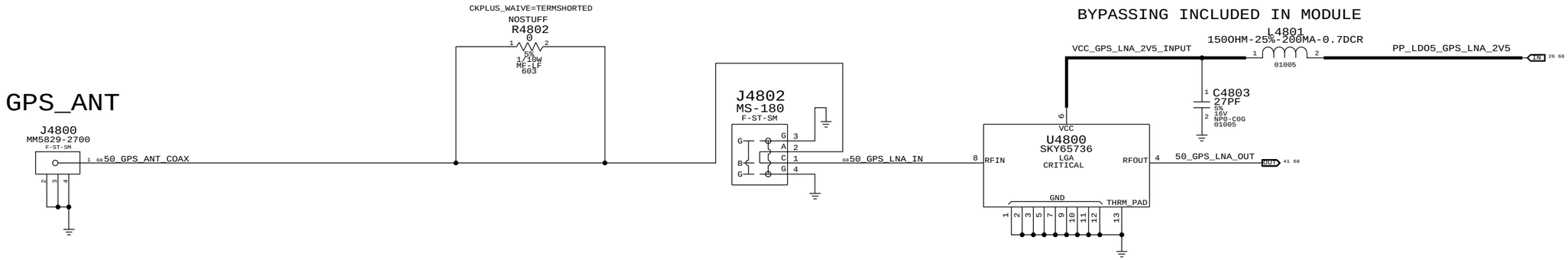
RX DIVERSITY



NEED TO UPDATE

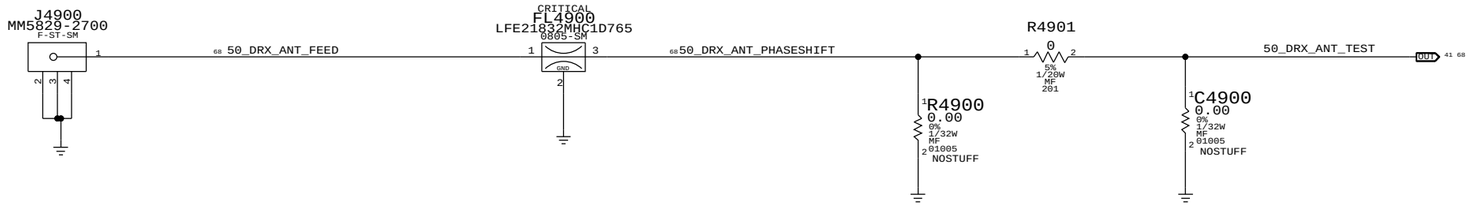
BAND	DRX_ASM_V4	DRX_ASM_V3	DRX_ASM_V2	DRX_ASM_V1
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH
SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES				

GPS

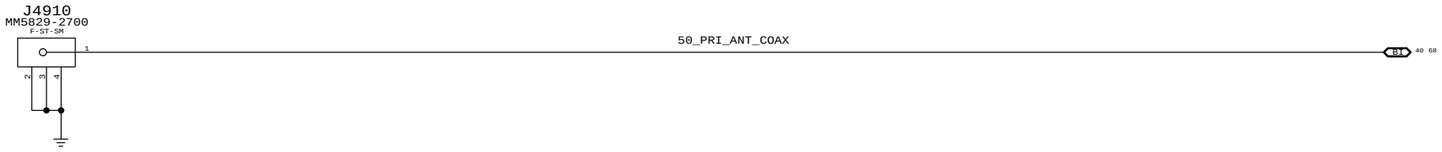


ANTENNA FEEDS

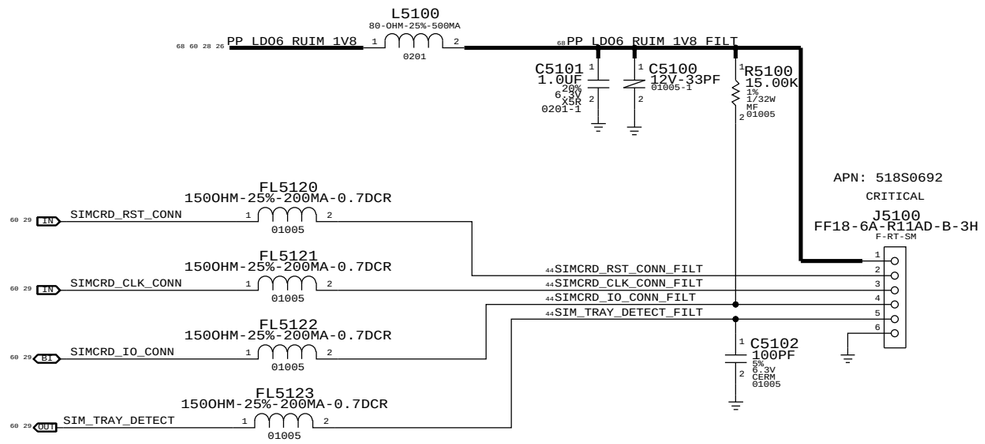
DRX_ANT COAX



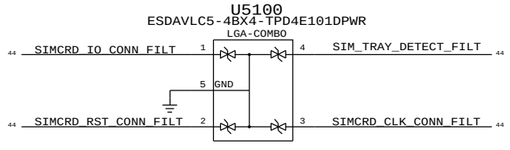
PRI_ANT COAX



SIM CARD FLEX CONN

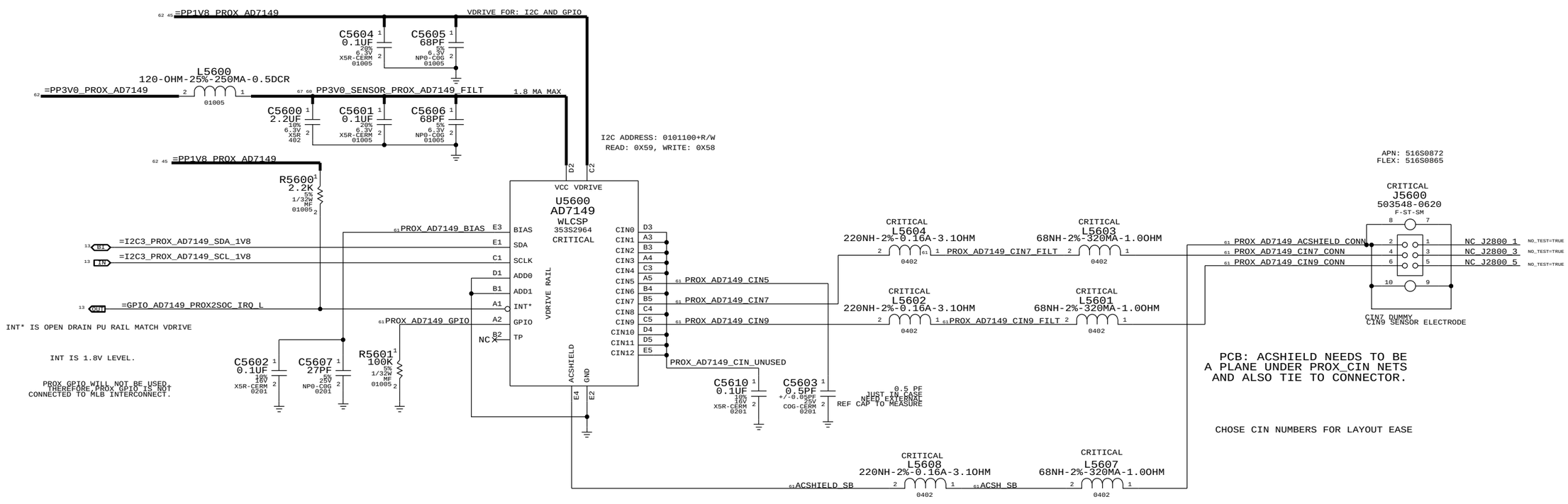


SIM CARD ESD PROTECTION



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0130	377S0159	?	U5100	RDAR://PROBLEM/12840016

PROX SENSOR



PCB: ENSURE ACSHIELD PLANE UNDER
U3200, NO GND PLANE NEAR PROX_CIN NETS..

WIFI/BT: MODULE

MODULE ISOLATION

XW5890 SHORT-10L-0.25MM-SM: PMU_GPIO_WLAN_REG_ON (IN, 61 57) → PMU_GPIO_WLAN_REG_ON_R (46 60)
XW5891 SHORT-10L-0.25MM-SM: PMU_GPIO_BT_REG_ON (IN, 61 57) → PMU_GPIO_BT_REG_ON_R (46 60)
XW5892 SHORT-10L-0.25MM-SM: PMU_GPIO_CLK_32K_WLAN (IN, 64 57) → PMU_GPIO_CLK_32K_WLAN_R (46 60)
XW5893 SHORT-10L-0.25MM-SM: UART_WLAN2BB_LTE_COEX (OUT, 29 25) → UART_WLAN2BB_LTE_COEX_R (46 61)
XW5894 SHORT-10L-0.25MM-SM: UART_BB2WLAN_LTE_COEX (IN, 29 25) → UART_BB2WLAN_LTE_COEX_R (46 61)
XW5895 SHORT-10L-0.25MM-SM: UART2_WLAN2SOC_TX (OUT, 64 5) → UART2_WLAN2SOC_TX_R (46 61 64)
XW5896 SHORT-10L-0.25MM-SM: UART2_SOC2WLAN_TX (IN, 64 5) → UART2_SOC2WLAN_TX_R (46 61 64)
XW5897 SHORT-10L-0.25MM-SM: HSIC1_SOC2WLAN_HOST_RDY (IN, 64 5) → HSIC1_SOC2WLAN_HOST_RDY_R (46 61 64)

CRITICAL U5810 2.4-5.0GHZ SM
LOW(2.4GHZ) 3 ← RF_G_0_DIPLEXER (69)
HIGH(5.0GHZ) 1
ANT(COMMON) 5
GND 6 4 2

CRITICAL R5811 0.00 1% 1/20W MF 0201: RF_G_0_DIPLEXER (69) ↔ RF_G_0_BAW_ANT (69)

CRITICAL U5811 BAW-2436MHZ 885061 LCGA
IN 1 ← RF_G_0_BAW_ANT (69)
OUT 4 → RF_G_0_BAW_MOD (69)
GND 5 3 2

CRITICAL L5811 10NH-3%-250MA 0201: 1 ↔ 2
CRITICAL C5811 2.5NH+/-0.1NH-500MA 0201: 1 ↔ 2
CRITICAL L5810 8.2NH+/-3%-0.25A-0.7OHM 0201: 1 ↔ 2
CRITICAL C5810 0.5PF +/-0.05PF 25V C0G-CERM 201: 1 ↔ 2

RF_G_0_MATCH_MOD (69) ← CRITICAL C5810 0.5PF +/-0.05PF 25V C0G-CERM 201 (1 ↔ 2)

CRITICAL J5810 MM4829-2702 F-ST-SM
1 ← RF_G_ANT (69)
2 3 4

NOSTUFF C5817 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_ANT (69) ↔ GND
CRITICAL R5810 0.00 1% 1/20W MF 0201: RF_G_ANT (69) ↔ RF_G_ANT_MATCH_T (69)
NOSTUFF C5816 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_ANT_MATCH_T (69) ↔ GND

CRITICAL C5814 1.0NH+/-0.1NH-0.75A 0201: RF_A_0_DIPLEXER (69) ↔ RF_A_0_MATCH (69)
NOSTUFF C5815 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_A_0_DIPLEXER (69) ↔ GND
CRITICAL C5813 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_0_MATCH (69) ↔ GND

CRITICAL J5820 MM4829-2702 F-ST-SM
1 ← RF_1_ANT (69)
2 3 4

NOSTUFF C5827 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_1_ANT (69) ↔ GND
CRITICAL R5820 0.00 1% 1/20W MF 0201: RF_1_ANT (69) ↔ RF_1_ANT_MATCH_T (69)
NOSTUFF C5826 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_1_ANT_MATCH_T (69) ↔ GND

CRITICAL U5820 DPX205850DT-9038A1SJ SM
COM 5 ← RF_1_ANT_MATCH_T (69)
HI 1
LO 3
GND 6 4 2

CRITICAL C5821 0.00 1% 1/20W MF 0201: RF_G_1_DIPLEXER (69) ↔ RF_G_1_MATCH_MOD (69)
NOSTUFF C5822 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_1_DIPLEXER (69) ↔ GND
CRITICAL C5820 1.0PF +/-0.05PF 25V C0G-CERM 0201: RF_G_1_MATCH_MOD (69) ↔ GND

CRITICAL C5824 0.8NH-+/-0.1NH-0.8MA 0201: RF_A_1_DIPLEXER (69) ↔ RF_A_1_MATCH (69)
CRITICAL C5825 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_1_DIPLEXER (69) ↔ GND
NOSTUFF C5823 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_1_MATCH (69) ↔ GND

62 =PPVCC_MAIN_WLAN
C5880 10UF 20% 6.3V CERM-X5R 0402-2
C5881 10UF 20% 6.3V CERM-X5R 0402-2
C5882 10UF 20% 6.3V CERM-X5R 0402-2

=PP3V3_S2R_WIFI_PA (61 62)
C5800 4.7UF 20% 6.3V X5R-CERM1 402
C5801 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL U5800 WIFI-BT-DOPPELBOCK LGA

	16	VBAT
	17	VBAT
	70	RF_VCC_FEM
	71	RF_VCC_FEM
PMU_GPIO_CLK_32K_WLAN_R (60 46)	33	CLK_32K
PMU_GPIO_WLAN_REG_ON_R (60 46)	4	WL_REG_ON
PMU_GPIO_BT_REG_ON_R (60 46)	3	BT_REG_ON
JTAG_WLAN_SEL (61)	23	JTAG_SEL
HSIC1_WLAN_DATA (64 61 4 BI)	13	HSIC_DATA
HSIC1_WLAN_STB (64 61 4 BI)	14	HSIC_STROBE
NC	7	SDIO_CLK
NC	6	SDIO_CMD
NC	8	SDIO_DATA0
NC	9	SDIO_DATA1
NC	10	SDIO_DATA2
NC	11	SDIO_DATA3
NC	77	RF_SW_CTRL11
NC	47	I2SWS
NC	36	I2SDO
NC	48	I2SDI
NC	39	I2SCLK
	67	RF_A_0
	79	RF_A_1
	62	RF_G_0
	74	RF_G_1
BT_GPIO5/LTE_COEX_UART_TX	51	UART_WLAN2BB_LTE_COEX_R (46 61)
BT_GPIO4/LTE_COEX_UART_RX	50	UART_BB2WLAN_LTE_COEX_R (46 61)
BT_GPIO1/HOSTWAKE	55	PMU_GPIO_BT_HOST_WAKE (OUT 57)
BT_GPIO0/BTWAKE	56	GPIO_BT_WAKE (IN 5 61)
BT_UART_RXD	37	UART1_SOC2BT_TX (IN 5 64)
BT_UART_TXD	38	UART1_BT2SOC_TX (OUT 5 64)
BT_UART_RTS*	36	UART1_BT2SOC_RTS_L (OUT 5 64)
BT_UART_CTS*	39	UART1_SOC2BT_RTS_L (IN 5 64)
BT_PCM_CLK	41	I2S4_SOC2BT_BCLK (IN 5 64)
BT_PCM_SYNC	42	I2S4_SOC2BT_LRCK (IN 5 64)
BT_PCM_OUT	43	I2S4_BT2SOC_DATA (OUT 5 64)
BT_PCM_IN	44	I2S4_SOC2BT_DATA (IN 5 64)
GPIO0/WL_HOST_WAKE	22	PMU_GPIO_WLAN_HOST_WAKE (OUT 57)
GPIO1/HOST_READY	20	HSIC1_SOC2WLAN_HOST_RDY_R (46 61 64)
GPIO2/WL_TCK	27	TP_JTAG_WLAN_TCK (61 64)
GPIO3/WL_TMS	28	JTAG_WLAN_TMS_TX_BLANK (64 61)
GPIO4/WL_TDI	26	JTAG_WLAN_TDI_OSCAR_A (64 61)
GPIO5/WL_TDO	24	JTAG_WLAN_TDO_OSCAR_B (64 61)
GPIO12/WL_TRST*	25	TP_JTAG_WLAN_TRST_L (61 64)
GPIO9/AGG_CHANNEL	19	NC
GPIO10/HSIC_DEVICE_READY	1	HSIC1_WLAN2SOC_DEVICE_RDY (OUT 5 61 64)
GPIO11/HSIC_RESUME	2	HSIC1_WLAN2SOC_REMOTE_WAKE (OUT 5 61 64)
GPIO15/WLAN_UART_TX	52	UART2_WLAN2SOC_TX_R (46 61 64)
GPIO14/WLAN_UART_RX	53	UART2_SOC2WLAN_TX_R (46 61 64)
GPIO6	30	NC
GPIO7	29	WLAN_GPIO7
GPIO8	31	NC
VIO	35	=PP1V8_S2R_VDDIO_WLAN_BT (46 62)
DUMMY	57	NC
GND_SIGNAL	5	GND_SIGNAL
GND_SIGNAL	12	GND_SIGNAL
GND_SIGNAL	15	GND_SIGNAL
GND_SIGNAL	18	GND_SIGNAL
GND_SIGNAL	21	GND_SIGNAL
GND_SIGNAL	32	GND_SIGNAL
GND_SIGNAL	34	GND_SIGNAL
GND_SIGNAL	40	GND_SIGNAL
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GND_SIGNAL	58	GND_SIGNAL
GND_SIGNAL	59	GND_SIGNAL
GND_SIGNAL	60	GND_SIGNAL
GND_SIGNAL	61	GND_SIGNAL
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GND_SIGNAL	65	GND_SIGNAL
GND_SIGNAL	66	GND_SIGNAL
GND_SIGNAL	68	GND_SIGNAL
GND_SIGNAL	69	GND_SIGNAL
GND_SIGNAL	72	GND_SIGNAL
GND_SIGNAL	73	GND_SIGNAL
GND_SIGNAL	75	GND_SIGNAL
GND_SIGNAL	76	GND_SIGNAL
GND_SIGNAL	78	GND_SIGNAL
GND_SIGNAL	80	GND_SIGNAL
GND_SIGNAL	81	GND_SIGNAL
GND_SIGNAL	82	GND_SIGNAL
GND_SIGNAL	83	GND_SIGNAL
GND_SIGNAL	84	GND_SIGNAL
GND_SIGNAL	85	GND_SIGNAL
GND_SIGNAL	86	GND_SIGNAL
GND_SIGNAL	87	GND_SIGNAL
GND_SIGNAL	88	GND_SIGNAL

R5804 0.00 1% 1/32W MF 01005: WLAN_TX_BLANK (IN 29)
R5801 0.00 1% 1/32W MF 01005: OSCAR2RADIO_CONTEXT_A (IN 19 29)
R5802 0.00 1% 1/32W MF 01005: OSCAR2RADIO_CONTEXT_B (IN 19 29)
=PP1V8_S2R_VDDIO_WLAN_BT (46 62)
R5803 10K 5% 1/32W MF 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104	?		RDAR://PROBLEM/12840267

DZ6000,DZ6001,DZ6002,DZ6003,DZ6090

=PP3V0_S2R_TRISTAR
C6030 1.0UF 20% 6.3V X5R 0201-1
C6035 0.22UF 20% 6.3V X5R 0201
C6040 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP3V3_ACC
C6042 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C6032 0.22UF 20% 6.3V X5R 0201
=PP1V8_S2R_TRISTAR
C6031 0.22UF 20% 6.3V X5R 0201
C6041 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
PPVBUS_PROT
C6043 8.2PF +/-0.25PF 25V NP0-C0G 0201
C6034 1UF 10% 25V X5R 0402
C6045 1UF 10% 25V X5R 0402

U6000
CBTL1610A1UK
WLCSP

VDD_1V8	F3		
VDD_3V0	F4		
ACC_PWR	D5		
DIG_DP	C3	MIKEY_TS_P	BI
DIG_DN	C4	MIKEY_TS_N	BI
USB1_DP	A1	USB_BB_P	BI
USB1_DN	B1	USB_BB_N	BI
BRICK_ID	C2	PMU_USB_BRICKID	OUT
USB0_DP	A3	USB_SOC_P	BI
USB0_DN	B3	USB_SOC_N	BI
UART0_TX	E2	UART6_TS_ACC_TXD	IN
UART0_RX	E1	UART6_TS_ACC_RXD	OUT
UART1_TX	F2	UART0_SOC_TXD	IN
UART1_RX	F1	UART0_SOC_RXD	OUT
UART2_TX	D2	UART3_BB2SOC_TX	IN
UART2_RX	D1	UART3_SOC2BB_TX	OUT
JTAG_CLK	A5	JTAG_SOC_TCK_R	
JTAG_DIO	B5	JTAG_SOC_TMS_R	
P_IN	F6		
ACC1	C5	PPOUT_E75_ACC_ID1	
ACC2	E5	PPOUT_E75_ACC_ID2	
DP1	A2	E75_DPAIR1_P	
DN1	B2	E75_DPAIR1_N	
DP2	A4	E75_DPAIR2_P	
DN2	B4	E75_DPAIR2_N	
CON_DET_L	E3	TS_E75_ACC_DET_L	
POW_GATE_EN*	D6	OVP_SW_EN_L	OUT
SWITCH_EN	E4	RESET_SOC_L	IN
HOST_RESET	B6	TS2PMU_RESET_IN	OUT
SDA	D3	I2C2_SDA_1V8	OUT
SCL	D4	I2C2_SCL_1V8	IN
INT	C6	GPIO_TS2SOC2PMU_INT	OUT
BYPASS	E6	BYPASS_U5900	
DVSS	F5		
DVSS	C1		
DVSS	A6		

TO BB USB
ACCESSORY USB
ACCESSORY UART
AP DEBUG UART
BB DEBUG UART
(T'S OFF TO SOC UART3)

R6030 0.00 5% 1/32W MF 01005 — JTAG_SOC_TCK
R6031 0.00 5% 1/32W MF 01005 — JTAG_SOC_TMS
C6033 1.0UF 20% 6.3V X5R 0201-1

TRISTAR 2:
AS OF 10/11/12 STILL PLAN TO STUFF CAP EVEN WITH TRISTAR2
RDAR://PROBLEM/12580126

XW6000 SHORT-10L-0.25MM-SM — L81_MBUS_REF
PLACE_NEAR=U6000.F5:5MM

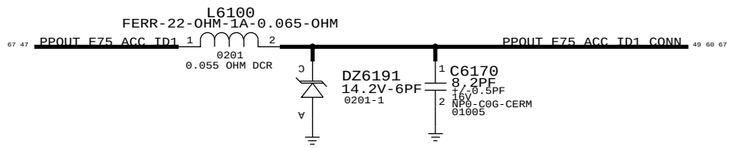
TRISTAR 2:
FOR PULSED CON_DET_L SUPPORT
NOSTUFF R6080, STUFF R6081

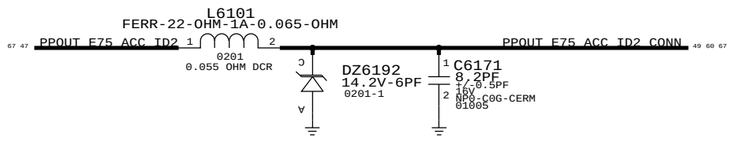
NOSTUFF R6080 0.00 5% 1/32W MF 01005 — PMU_E75_ACC_DET_L
R6081 0.00 5% 1/32W MF 01005

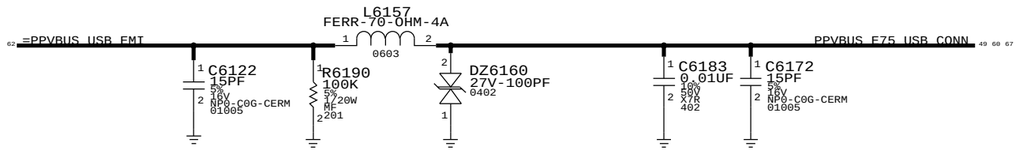
CRITICAL L6030 90-OHM-50MA TCM0605-1
CRITICAL L6031 90-OHM-50MA TCM0605-1
E75_DPAIR1_CONN_P
E75_DPAIR1_CONN_N
E75_DPAIR2_CONN_P
E75_DPAIR2_CONN_N

CRITICAL DZ6000 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6001 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6002 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6003 ESD0P2RF-02LS TSSLP-2-1 0.4PF

PPVCC_MAIN
NOSTUFF R6091 100K 5% 1/32W MF 01005
C6091 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
R6090 10K 5% 1/32W MF 01005
E75_ACC_DET_R_L
FL6090 120-OHM-25%-250MA-0.5DCR 01005
E75_ACC_DET_CONN_L
NOSTUFF C6090 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
CRITICAL D6090 SM-201 DSF01S30SC
CRITICAL DZ6090 ESD0P2RF-02LS TSSLP-2-1



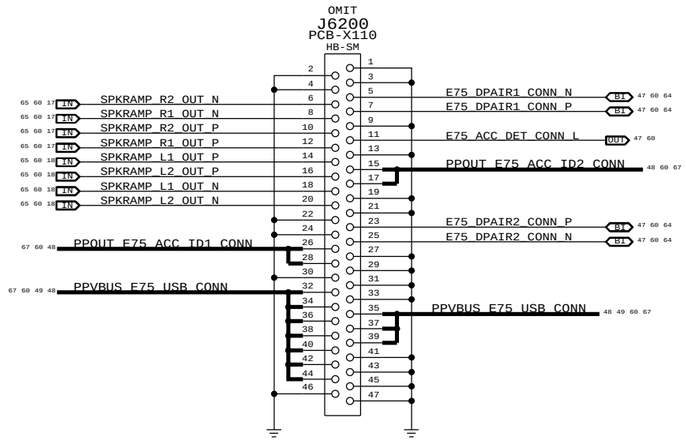




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ6160	RDAR:8370432
155S0320	155S0513		L6100,L6101	RDAR://PROBLEM/9625601
155S0741	155S0397		L6157	RDAR://PROBLEM/11238851

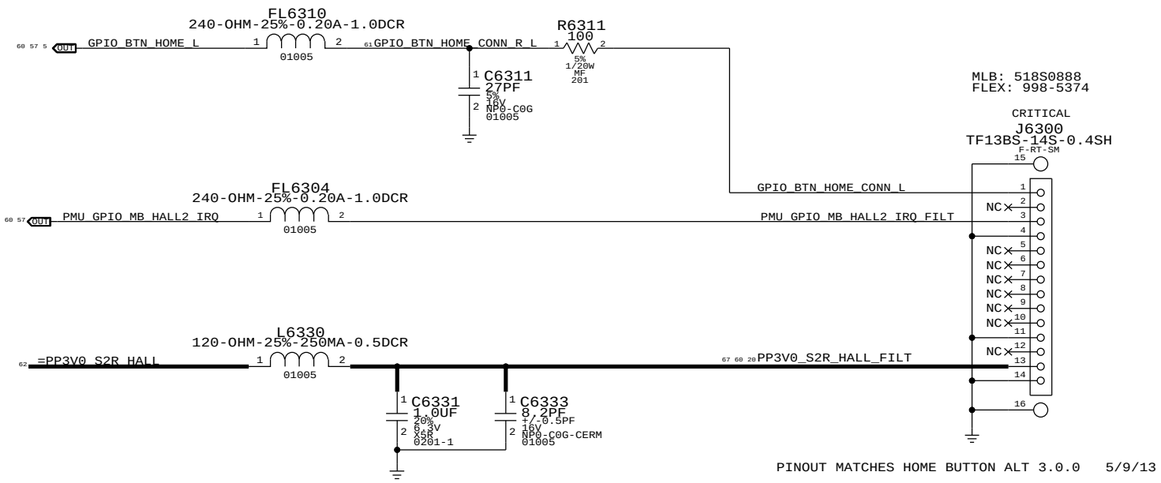
IO FLEX HOTBAR PADS

MLB 998-5877
FLEX 998-5876

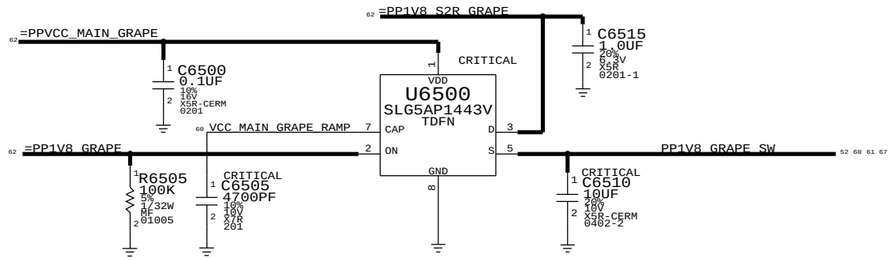


PINOUT MATCHES IO_FLEX 4.2.0 3/12/13

HOME BUTTON FILTERS



GRAPE CONNECTOR SUPPORT



LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2300 IN CASE OF SHORTED CONDITION

CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

MASTER CUMULUS

=PP5V25_GRAPE
C6602 1UF 10% 25V X5R 0402
C6609 100PF 5% 6.3V CERM 01005
PP1V8_GRAPE_SW
C6603 0.1UF 10% 16V X5R-CERM 0201
CUMULUS_M_VDDCORE
CUMULUS_M_VDDANA
C6600 2.2UF 10% 10V X5R-CERM 0402
C6601 2.2UF 10% 10V X5R-CERM 0402
C6604 4.7UF 20% 10V X5R-CERM 0402
C6605 0.1UF 10% 16V X5R-CERM 0201
C6606 100PF 5% 6.3V CERM 01005

U6600
CUMULUS-C1
WLBGA
CRITICAL

MT_PANEL_IN<15>	B9	IN0_0	
MT_PANEL_IN<16>	B8	IN1_0	
MT_PANEL_IN<17>	A9	IN2_0	
MT_PANEL_IN<18>	B7	IN3_0	
MT_PANEL_IN<19>	B6	IN4_0	
MT_PANEL_IN<20>	A8	IN5_0	
MT_PANEL_IN<21>	B5	IN6_0	
MT_PANEL_IN<22>	B4	IN7_0	
MT_PANEL_IN<23>	A7	IN8_0	
MT_PANEL_IN<24>	B3	IN9_0	
MT_PANEL_IN<25>	A6	IN10_0	
MT_PANEL_IN<26>	A3	IN11_0	
MT_PANEL_IN<27>	A5	IN12_0	
MT_PANEL_IN<28>	A4	IN13_0	
MT_PANEL_IN<29>	B2	IN14_0	
NC_CUMULUS_M_IN14_1	A2	IN14_1	
SPI2_GRAPE_CS_L	E4	H_CS*	
GPIO_GRAPE2SOC_IRQ_L	F1	H_INT*	
SPI2_GRAPE_SCLK	D3	H_SCLK	
SPI2_GRAPE_MOSI	D2	H_SDI	
SPI2_GRAPE_MISO	E1	H_SDO	
TP_JTAG_CUMULUS_M_TCK	C4	JTAG_TCK	
TP_JTAG_CUMULUS_M_TDI	C3	JTAG_TDI	
TP_JTAG_CUMULUS_M_TDO	E2	JTAG_TDO	
JTAG_CUMULUS_M_TMS	C6	JTAG_TMS	
CUMULUS_M_BCFG_RTCK	E3	BCFG_RTCK	
CLK_32K_SOC2CUMULUS	D1	CLKIN/RESET*	
GPIO_SOC2GRAPE_RESET_L	D9	RSTOVR*	

VSTM_0	E9	MT_PANEL_OUT<0>	
VSTM_1	E5	MT_PANEL_OUT<1>	
VSTM_2	F7	MT_PANEL_OUT<2>	
VSTM_3	E6	MT_PANEL_OUT<3>	
VSTM_4	E7	MT_PANEL_OUT<4>	
VSTM_5	F8	MT_PANEL_OUT<5>	
VSTM_6	G9	MT_PANEL_OUT<6>	
VSTM_7	D6	MT_PANEL_OUT<7>	
VSTM_8	D7	MT_PANEL_OUT<8>	
VSTM_9	D8	MT_PANEL_OUT<9>	
VSTM_10	F9	MT_PANEL_OUT<10>	
VSTM_11	D5	MT_PANEL_OUT<11>	
VSTM_12	F6	MT_PANEL_OUT<12>	
VSTM_13	F5	MT_PANEL_OUT<13>	
VSTM_14	G4	MT_PANEL_OUT<14>	
VSTM_15	E8	MT_PANEL_OUT<15>	
VSTM_16	G8	MT_PANEL_OUT<16>	
VSTM_17	G7	MT_PANEL_OUT<17>	
VSTM_18	G6	MT_PANEL_OUT<18>	
VSTM_19	G5	MT_PANEL_OUT<19>	
GPIO_1/CK	G1	CUMULUS_MS_CK	
GPIO_2/SD	D4	CUMULUS_MS_SD	
GPIO_3	F2	DISPLAY_SYNC	
GPIO_4	F3	NC_ESD_SENSE_R	
TM_ACS*	C2	NC_CUMULUS_M_TM_ACS_L	
TM_OVR	G3		

R6600 4.7K 1% 1/32W MF 01005
R6601 4.7K 1% 1/32W MF 01005
R6603 4.7K 1% 1/32W MF 01005
R6604 100K 5% 1/32W MF 01005
GND
C7 C9 G2

SLAVE CUMULUS

=PP5V25_GRAPE
C6652 1UF 10% 25V X5R 0402
PP1V8_GRAPE_SW
C6653 0.1UF 10% 16V X5R-CERM 0201
CUMULUS_S_VDDCORE
CUMULUS_S_VDDANA
C6650 2.2UF 10% 10V X5R-CERM 0402
C6651 2.2UF 10% 10V X5R-CERM 0402
C6654 0.1UF 10% 16V X5R-CERM 0201
C6656 100PF 5% 6.3V CERM 01005

U6650
CUMULUS-C1
WLBGA
CRITICAL

MT_PANEL_IN<0>	B9	IN0_0	
MT_PANEL_IN<1>	B8	IN1_0	
MT_PANEL_IN<2>	A9	IN2_0	
MT_PANEL_IN<3>	B7	IN3_0	
MT_PANEL_IN<4>	B6	IN4_0	
MT_PANEL_IN<5>	A8	IN5_0	
MT_PANEL_IN<6>	B5	IN6_0	
MT_PANEL_IN<7>	B4	IN7_0	
MT_PANEL_IN<8>	A7	IN8_0	
MT_PANEL_IN<9>	B3	IN9_0	
MT_PANEL_IN<10>	A6	IN10_0	
MT_PANEL_IN<11>	A3	IN11_0	
MT_PANEL_IN<12>	A5	IN12_0	
MT_PANEL_IN<13>	A4	IN13_0	
MT_PANEL_IN<14>	B2	IN14_0	
NC_CUMULUS_S_IN14_1	A2	IN14_1	
TP_CUMULUS_S_H_CS_L	E4	H_CS*	
NC_CUMULUS_S_H_INT_L	F1	H_INT*	
TP_CUMULUS_S_H_SCLK	D3	H_SCLK	
TP_CUMULUS_S_H_SDI	D2	H_SDI	
TP_CUMULUS_S_H_SDO	E1	H_SDO	
NC_JTAG_CUMULUS_S_TCK	C4	JTAG_TCK	
NC_JTAG_CUMULUS_S_TDI	C3	JTAG_TDI	
NC_JTAG_CUMULUS_S_TDO	E2	JTAG_TDO	
JTAG_CUMULUS_S_TMS	C6	JTAG_TMS	
CUMULUS_S_BCFG_RTCK	E3	BCFG_RTCK	
CLK_32K_SOC2CUMULUS	D1	CLKIN/RESET*	
GPIO_SOC2GRAPE_RESET_L	D9	RSTOVR*	

VSTM_0	E9	MT_PANEL_OUT<20>	
VSTM_1	E5	MT_PANEL_OUT<21>	
VSTM_2	F7	MT_PANEL_OUT<22>	
VSTM_3	E6	MT_PANEL_OUT<23>	
VSTM_4	E7	MT_PANEL_OUT<24>	
VSTM_5	F8	MT_PANEL_OUT<25>	
VSTM_6	G9	MT_PANEL_OUT<26>	
VSTM_7	D6	MT_PANEL_OUT<27>	
VSTM_8	D7	MT_PANEL_OUT<28>	
VSTM_9	D8	MT_PANEL_OUT<29>	
VSTM_10	F9	MT_PANEL_OUT<30>	
VSTM_11	D5	MT_PANEL_OUT<31>	
VSTM_12	F6	MT_PANEL_OUT<32>	
VSTM_13	F5	MT_PANEL_OUT<33>	
VSTM_14	G4	MT_PANEL_OUT<34>	
VSTM_15	E8	MT_PANEL_OUT<35>	
VSTM_16	G8	MT_PANEL_OUT<36>	
VSTM_17	G7	MT_PANEL_OUT<37>	
VSTM_18	G6	MT_PANEL_OUT<38>	
VSTM_19	G5	MT_PANEL_OUT<39>	
GPIO_1/CK	G1	CUMULUS_MS_CK	
GPIO_2/SD	D4	CUMULUS_MS_SD	
GPIO_3	F2	NC_AG_TEST_GND_SNS	
GPIO_4	F3	NC_AG_TEST_GND_DRV	
TM_ACS*	C2	NC_CUMULUS_S_TM_ACS_L	
TM_OVR	G3		

R6650 4.7K 1% 1/32W MF 01005
R6651 4.7K 1% 1/32W MF 01005
GND
C7 C9 G2

PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

CRITICAL

J6620
AA03-S042VA1
F-ST-SM

MT_PANEL_OUT<12>	3	4	MT_PANEL_OUT<13>		
MT_PANEL_OUT<11>	5	6	MT_PANEL_OUT<14>		
MT_PANEL_OUT<10>	7	8	MT_PANEL_OUT<15>		
MT_PANEL_OUT<9>	9	10	MT_PANEL_OUT<16>		
MT_PANEL_OUT<8>	11	12	MT_PANEL_OUT<17>		
MT_PANEL_OUT<7>	13	14	MT_PANEL_OUT<18>		
MT_PANEL_OUT<6>	15	16	MT_PANEL_OUT<19>		
MT_PANEL_OUT<5>	17	18	MT_PANEL_OUT<20>		
MT_PANEL_OUT<4>	19	20	MT_PANEL_OUT<21>		
MT_PANEL_OUT<3>	21	22	MT_PANEL_OUT<22>		
MT_PANEL_OUT<2>	23	24	MT_PANEL_OUT<23>		
MT_PANEL_OUT<1>	25	26	MT_PANEL_OUT<24>		
MT_PANEL_OUT<0>	27	28	MT_PANEL_OUT<25>		
MT_PANEL_OUT<26>	29	30	MT_PANEL_OUT<39>		
MT_PANEL_OUT<27>	31	32	MT_PANEL_OUT<38>		
MT_PANEL_OUT<28>	33	34	MT_PANEL_OUT<37>		
MT_PANEL_OUT<29>	35	36	MT_PANEL_OUT<36>		
MT_PANEL_OUT<30>	37	38	MT_PANEL_OUT<35>		
MT_PANEL_OUT<31>	39	40	MT_PANEL_OUT<34>		
MT_PANEL_OUT<32>	41	42	MT_PANEL_OUT<33>		
	43	44			
	45	46			

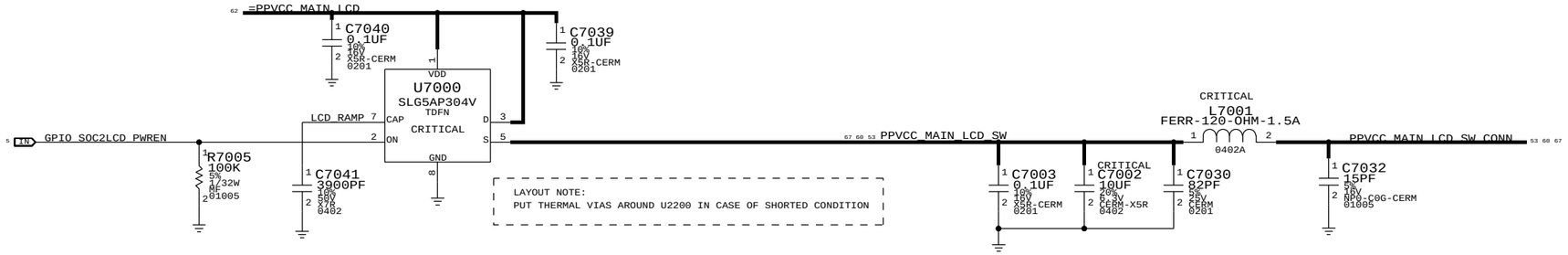
PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

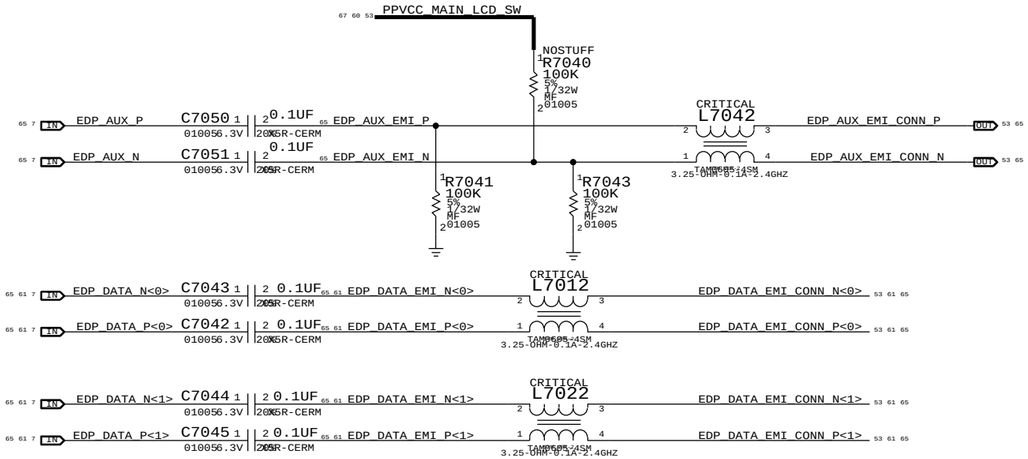
CRITICAL

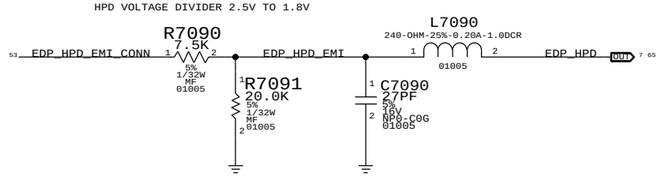
J6640
AA03-S034VA1
F-ST-SM

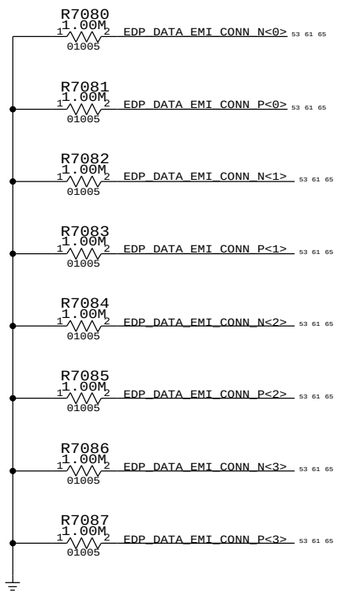
MT_PANEL_IN<14>	3	4	MT_PANEL_IN<29>		
MT_PANEL_IN<13>	5	6	MT_PANEL_IN<28>		
MT_PANEL_IN<12>	7	8	MT_PANEL_IN<27>		
MT_PANEL_IN<11>	9	10	MT_PANEL_IN<26>		
MT_PANEL_IN<10>	11	12	MT_PANEL_IN<25>		
MT_PANEL_IN<9>	13	14	MT_PANEL_IN<24>		
MT_PANEL_IN<8>	15	16	MT_PANEL_IN<23>		
MT_PANEL_IN<17>	17	18	MT_PANEL_IN<22>		
MT_PANEL_IN<6>	19	20	MT_PANEL_IN<21>		
MT_PANEL_IN<5>	21	22	MT_PANEL_IN<20>		
MT_PANEL_IN<4>	23	24	MT_PANEL_IN<19>		
MT_PANEL_IN<3>	25	26	MT_PANEL_IN<18>		
MT_PANEL_IN<2>	27	28	MT_PANEL_IN<7>		
MT_PANEL_IN<16>	29	30	MT_PANEL_IN<0>		
MT_PANEL_IN<15>	31	32	MT_PANEL_IN<1>		
	33	34			
	35	36			
	37	38			

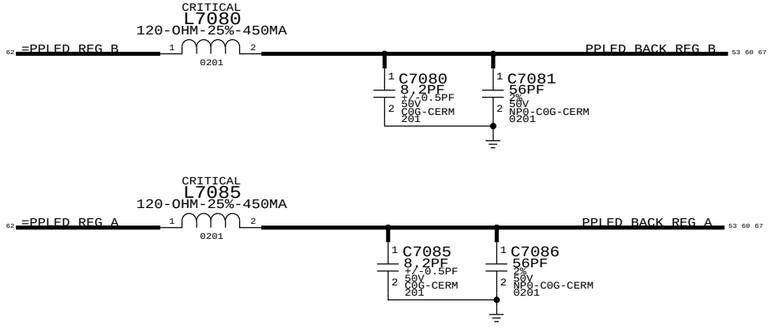
EDP CONNECTOR SUPPORT





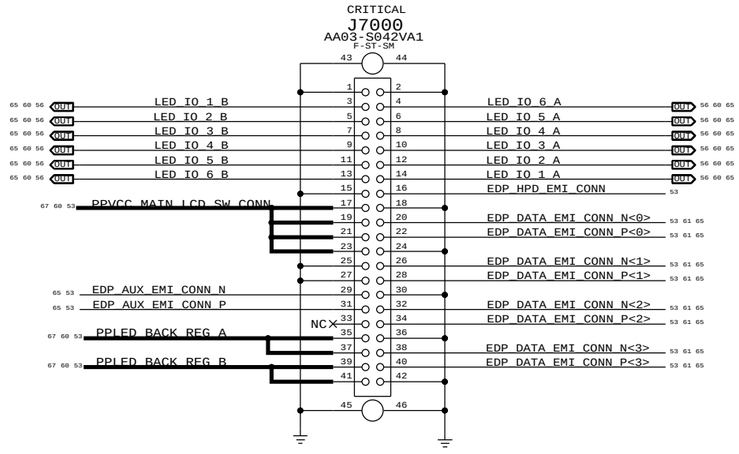






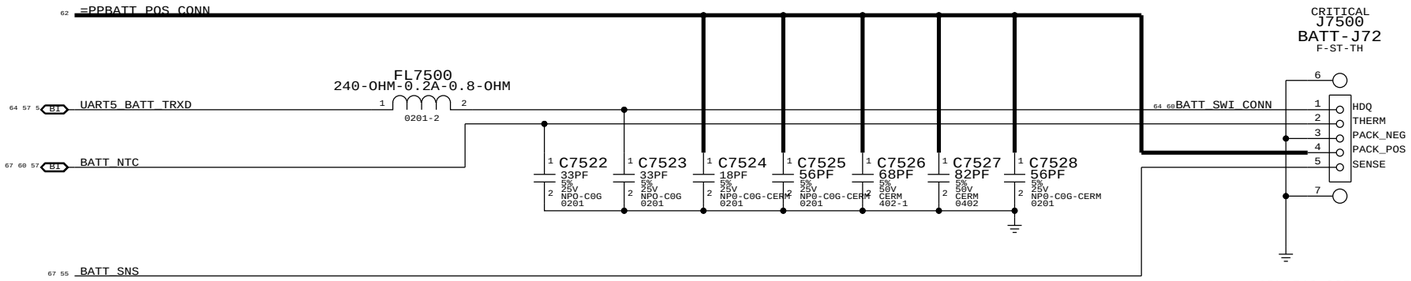
EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823	?		RDAR://PROBLEM/11282371

FL7500,L1920



APN:516-0254

PLACEMENT_NOTE=PLACE NEAR L8225.1

CRITICAL C8140 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM
CRITICAL C8141 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM

VCC_MAIN BYPASS
PLACE TWO 10UF CAP
AT EACH VDD INPUT

CRITICAL C8150–C8159 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8160–C8172 10UF 20% 6.3V CERM-X5R 0402

PPVCC_MAIN 47 55 56 57 58 60 62 67
CRITICAL C8144 1.0UF 20% 6.3V CERM 0201-1
C8142 82PF 5% 25V CERM 0201
CRITICAL C8143 18PF 5% 25V NP0,C0G-CERM 0201

USB REVERSE VOLTAGE PROTECTION

PPVCC_MAIN 67 62 60 58 57 56 55 47
OVP_SW_EN_L 55 47
NOSTUFF R8170 4.7K 5% 1/20W MF 201
CRITICAL Q8104 FDMC6683 MLP3.3X3.3
RDSON=0.0136@VGS=-2.5V
ID=12.0A
PPBATT_VCC 67 62 60 58
ACT_DIO
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=ANLG

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

NOSTUFF R8116 470K 1% 1/20W MF 201
CRITICAL Q8123 FDMC6676BZ MLP3.3X3.3
PPVBUS_USB_DCIN 67 62 60
CRITICAL DZ8120 BZT52C10LP LLP
NOTE: 10V ZENER
VBUS_PROT_G 60
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=ANLG
R8130 220K 1% 1/20W MF 201

SWITCHER

CRITICAL L8112 2.2UH-20%-5.6A-0.03OHM PILE101D-SM DCR=30MOHM MAX
SW_CHGA 67 61
CRITICAL D8100 SOD-123W PMEG4030ER
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
NET_SPACING_TYPE=PWR
DIDT=TRUE
SWITCH_NODE=TRUE
PLACE_NEAR=U8100.R17:2MM
R8172 0 5% 1/20W MF 201
BATT_SNS 67 54
BATT_SNS_R 67
NOSTUFF C8149 0.022UF 10% 25V X7R 0402
R8173 499 1% 1/20W MF 201
PLACE_NEAR=U8100.R17:10MM
LAYOUT NOTE -
R8172- PLACE NEAR PMU
R8149- PLACE NEAR PMU
R8173- PLACE NEAR PMU

XW8114 SHORT-0201
USB_VBUS_DETECT 67 4
CRITICAL C8148 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8147 4.7UF 10% 35V X5R-CERM 0603
PLACE_NEAR=U8100.F18:2MM
PLACE_NEAR=U8100.L18:2MM
PMU_VCENTER 67 60
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
VOLTAGE=6.0V
LAYOUT NOTE: PLACE RIGHT AT THE PIN

PPVBUS_PROT 67 60 47
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
VOLTAGE=6.0V
CRITICAL C8145 2.2UF 10% 25V X5R-CERM 603
PLACE_NEAR=U8100.G16:2MM
LAYOUT NOTE: PLACE RIGHT AT THE PIN

R8146 4.7K 5% 1/20W MF 201
OVP_SW_EN_L 55 47 — OVP_SW_EN_L_R
NOSTUFF C8146 0.01UF 10% 25V X5R-CERM 0201
LAYOUT NOTE:
R8146, C8146 CAN BE
ANYWHERE BET.TRISTAR
AND PMU

TP_HV_CHG_EN
=PPVCC_MAIN_CPU 62 55
=PPVCC_MAIN_GPU 62 55
=PPVCC_MAIN_SOC 62 55
PPVCC_MAIN 67 62 60 58 57 56 55 47

OMIT_TABLE
U8100 D2089A0 FCBGA
SYM 1 OF 4

G19	CHG_LX0
H19	CHG_LX1
J19	CHG_LX2
K19	CHG_LX3
R17	VBAT
P17	IBAT_S
M19	IBAT0
N19	IBAT1
P19	IBAT2
R19	IBAT3
N17	ACT_DIO
F18	VCENTER
F19	VCENTER
G18	VCENTER
H18	VCENTER
J18	VCENTER
K18	VCENTER
L18	VCENTER
L19	VCENTER
F16	VBUS
F17	VBUS
G16	VBUS
G17	VBUS
H16	VBUS
H17	VBUS
J17	VBUS
K16	VBUS
K17	VBUS
L16	VBUS
L17	VBUS
C16	VBUS_OVP_OFF
D17	HV_CHG_DIS
F1	VDD_BUCK0_01
F2	VDD_BUCK0_01
K1	VDD_BUCK0_01
K2	VDD_BUCK0_23
P1	VDD_BUCK1_01
P2	VDD_BUCK1_01
V1	VDD_BUCK1_01
V2	VDD_BUCK1_2
V3	VDD_BUCK1_2
U8	VDD_BUCK2
V8	VDD_BUCK2
A4	VDD_BUCK3
B4	VDD_BUCK3
A8	VDD_BUCK4
B8	VDD_BUCK4
U4	VDD_BUCK5
V4	VDD_BUCK5
B1	VDD_BUCK6
B2	VDD_BUCK6
B3	VDD_BUCK6
T16	VCC_MAIN_S
M18	VCC_MAIN
N18	VCC_MAIN
P18	VCC_MAIN
R18	VCC_MAIN

USB/BAT BUCK
VCC_MAIN SWITCHED POWER

E1	BUCK0_LX0
E2	BUCK0_LX0
G1	BUCK0_LX1
G2	BUCK0_LX1
J1	BUCK0_LX2
J2	BUCK0_LX2
L1	BUCK0_LX3
L2	BUCK0_LX3
H6	BUCK0_FB
N1	BUCK1_LX0
N2	BUCK1_LX0
R1	BUCK1_LX1
R2	BUCK1_LX1
U1	BUCK1_LX2
U2	BUCK1_LX2
M6	BUCK1_FB
U7	BUCK2_LX0
V7	BUCK2_LX0
P7	BUCK2_FB
A5	BUCK3_LX0
B5	BUCK3_LX0
E6	BUCK3_FB
A7	BUCK4_LX0
B7	BUCK4_LX0
E7	BUCK4_FB
U5	BUCK5_LX0
V5	BUCK5_LX0
P6	BUCK5_FB
C1	BUCK6_LX0
C2	BUCK6_LX0
F6	BUCK6_FB
A1	BUCK6_BYP0
A2	BUCK6_BYP1
A3	BUCK6_BYP2
B13	VBUCK3
B14	VBUCK3
C14	VBUCK3
A12	BUCK3_SW1
B12	BUCK3_SW1
C12	BUCK3_SW1
C13	BUCK3_SW1
A13	BUCK3_SW2
A14	BUCK3_SW3
B10	VBUCK4
B11	VBUCK4
C11	VBUCK4
A9	BUCK4_SW1
B9	BUCK4_SW1
C9	BUCK4_SW1
C10	BUCK4_SW2
A10	VPUMP
A11	VPUMP

CRITICAL L8100 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8101 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8102 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8103 1.0UH-3.51A-0.036OHM PILE25201D
XW8101 SM
CRITICAL L8104 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8105 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8106 1.0UH-3.51A-0.036OHM PILE25201D
XW8102 SM
CRITICAL L8107 1.0UH-3.51A-0.036OHM PILE25201D
XW8103 SM
CRITICAL L8108 1.0UH-3.51A-0.036OHM PILE25201D
CRITICAL L8109 1.0UH-3.51A-0.036OHM PILE25201D
XW8104 SM
CRITICAL L8109 1.0UH-3.51A-0.036OHM PILE25201D
XW8105 SM
CRITICAL L8110 1.0UH-3.7A-0.055OHM PILE20161D-SM
XW8106 SM
CRITICAL L8111 2.2UH-2.35A-0.073OHM PILE25201D
XW8107 SM

BUCK0_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK0_LX1 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK0_LX2 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK0_LX3 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK0_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK1_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK1_LX1 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK1_LX2 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK1_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK2_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK2_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK3_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK3_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK4_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK4_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK5_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK5_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM
BUCK6_LX0 MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=0.5 MM DIDT=TRUE SWITCH_NODE=TRUE
BUCK6_FB MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.20MM

PPVDD_CPU 60 62 67
CRITICAL C8100–C8104 15UF 20% 4V X5R 0402
CRITICAL C8105–C8109 15UF 20% 4V X5R 0402
CRITICAL C8110 15UF 20% 4V X5R 0402
CRITICAL C8111 15UF 20% 4V X5R 0402
PPVDD_GPU 60 62 67
CRITICAL C8112–C8116 15UF 20% 4V X5R 0402
CRITICAL C8117–C8120 15UF 20% 4V X5R 0402
ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PPVDD_SOC 60 62 67
CRITICAL C8121–C8123 15UF 20% 4V X5R 0402
ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PP1V8_S2R 55 56 60 62 67
CRITICAL C8124–C8126 15UF 20% 4V X5R 0402
ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PP1V2_S2R 55 56 60 62 67
CRITICAL C8127–C8129 15UF 20% 4V X5R 0402
ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PPVDD_SRAM 60 62 67
CRITICAL C8130–C8132 15UF 20% 4V X5R 0402
ADDITIONAL DISTRIBUTED 32UF (NO DERATING)
PP3V3_S2R 60 62 67
CRITICAL C81A0–C81A3 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C81A4–C81A7 10UF 20% 6.3V CERM-X5R 0402

PP1V8_S2R 55 56 60 62 67
PP1V8_SW1 57 59 60 62 67
PP1V8_SW2 60 62 67
PP1V8_S2R_SW3 60 62 67
PP1V2_S2R 55 56 60 62 67
PP1V2_SW1 60 62 67
PP1V2_S2R_SW2 60 62 67

PMU_VPUMP
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
VOLTAGE=4.6V
C8196 0.22UF 20% 6.3V CERM X5R 0201
C8135 1.0UF 20% 6.3V CERM X5R 0201-1
C8136 1UF 10% 6.3V CERM 402
C8137 1.0UF 20% 6.3V CERM X5R 0201-1
C81A8 1.0UF 20% 6.3V CERM X5R 0201-1
C8138 1.0UF 20% 6.3V CERM X5R 0201-1
C8139 1UF 10% 6.3V CERM 402
C81A9 1.0UF 20% 6.3V CERM X5R 0201-1

C8137 0201 OKAY IF GRAPE HAS EXT FET

=PPVCC_MAIN_CPU 62 55
CRITICAL C8175–C8181 10UF 20% 6.3V CERM-X5R 0402

=PPVCC_MAIN_GPU 62 55
CRITICAL C8182–C8186 10UF 20% 6.3V CERM-X5R 0402

=PPVCC_MAIN_SOC 62 55
CRITICAL C8187 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8188 10UF 20% 6.3V CERM-X5R 0402

NOTE: FOR NO BATTERY SITUATION
PPBATT_VCC 67 62 60 59
CRITICAL C8193 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8194 10UF 20% 6.3V CERM-X5R 0402
PPBATT_POS_RC 60
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
VOLTAGE=4.7V
R8100 0.5 1% 1/10W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8140,C8141	RDAR://PROBLEM/8967213

LDO INPUTS

PP1V8_S2R — 1 CAP PER PIN
- C8200 1UF 10% 6.3V CERM 402
- C8203 1UF 10% 6.3V CERM 402

PP1V2_S2R
- C8201 1UF 10% 6.3V CERM 402

PPVCC_MAIN (T18, B16, U9, U10, U14, U15, B15, B17, U16, T17)

CRITICAL L8225 4.7UH-3.4A-0.075OHM — PILE051D-SM-COMBO-J72 DCR=106MOHM MAX
- =PPVCC_MAIN_LED
- CRITICAL C8226 10UF 20% 6.3V CERM-X5R 0402

CRITICAL D8228 PMEG4010BEA SOD-323
- WLED_LX_A — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 MM
- NET_SPACING_TYPE=PWR, SWITCH_NODE=TRUE

(PPLED_OUT_A)

PPLED_OUT_A
- CRITICAL C8250 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8251 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8252 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8253 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8254 4.7UF 10% 35V X5R-CERM 0603
- C8259 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_1_A — R8270 1.00 1% 1/32W MF 01005
- C8271 56PF 2% 50V NP0-C0G-CERM 0201
- C8270 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_2_A — R8271 1.00 1% 1/32W MF 01005

LED_IO_3_A — R8272 1.00 1% 1/32W MF 01005
- C8273 56PF 2% 50V NP0-C0G-CERM 0201
- C8272 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_4_A — R8273 1.00 1% 1/32W MF 01005

LED_IO_5_A — R8274 1.00 1% 1/32W MF 01005
- C8275 56PF 2% 50V NP0-C0G-CERM 0201
- C8274 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_6_A — R8275 1.00 1% 1/32W MF 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789	?	L8225,L8255	RDAR://PROBLEM/13487208

WLED_LX_B — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20 MM

CRITICAL L8255 4.7UH-3.4A-0.075OHM — PILE051D-SM-COMBO-J72 DCR=106MOHM MAX
- =PPVCC_MAIN_LED
- CRITICAL C8256 10UF 20% 6.3V CERM-X5R 0402

CRITICAL D8258 PMEG4010BEA SOD-323

(PPLED_OUT_B)

PPLED_OUT_B
- CRITICAL C8260 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8261 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
- CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
- C8269 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_1_B — R8280 1.00 1% 1/32W MF 01005
- C8280 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_2_B — R8281 1.00 1% 1/32W MF 01005
- C8281 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_3_B — R8282 1.00 1% 1/32W MF 01005
- C8282 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_4_B — R8283 1.00 1% 1/32W MF 01005
- C8283 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_5_B — R8284 1.00 1% 1/32W MF 01005
- C8284 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_6_B — R8285 1.00 1% 1/32W MF 01005
- C8285 56PF 2% 50V NP0-C0G-CERM 0201

OMIT_TABLE

U8100 D2089A0 FCBGA SYM 2 OF 4

LDO INPUT / LDO
- VDD_LDO1_3_4 (T18)
- VDD_LDO2 (B16)
- VDD_LDO5 (U9)
- VDD_LDO6 (U10)
- VDD_LDO7 (U14)
- VDD_LDO8 (U15)
- VDD_LDO9 (B15)
- VDD_LDO10 (B17)
- VDD_LDO11 (U16)
- VDD_LDO13 (T17)

LCD BACKLIGHT / LCM/GRAPE
- WLED_LXA0 (C18)
- WLED_LXA1 (C19)
- VOUT_WLED_A (D16)
- WLED1_A (E14)
- WLED2_A (F14)
- WLED3_A (G14)
- WLED4_A (H14)
- WLED5_A (J14)
- WLED6_A (J16)
- WLED_LXB0 (E18)
- WLED_LXB1 (E19)
- VOUT_WLED_B (E16)
- WLED1_B (K14)
- WLED2_B (L14)
- WLED3_B (M14)
- WLED4_B (M16)
- WLED5_B (N14)
- WLED6_B (P14)

XTAL
- XTAL1 (V18)
- XTAL2 (V17)

LED_IO1_A_R … LED_IO6_A_R
LED_IO1_B_R … LED_IO6_B_R

LDO OUTPUTS

VLDO1	U19 (50MA; 2.5-3.3V)	PP3V0_SPARE1
VLDO2	A16 (100MA; 1.65-1.805V; BUCK3)	PP1V7_VA_VCP
VLDO3	U18 (50MA; 2.5-3.3V)	PP3V0_S2R_SENSOR
VLDO4	T19 (50MA; 2.5-3.3V)	PP3V0_ALS
VLDO5	V9 (1000MA; 2.5-3.6V)	PP3V0_UVLO
VLDO6	V10 (150MA; 2.5-3.6V)	PP3V3_ACC
VLDO7	V14 (300MA; 1.7-3.0V)	PP3V0_S2R_TRISTAR
VLDO8	V15 (300MA; 1.7-3.0V)	PP3V0_S2R_HALL
VLDO9	A15 (300MA; 1.2-3.0V)	PP1V3_CAM
VLDO10	A17 (150MA; 0.6-1.3V)	PP1V0_SOC
VLDO11	V16 (300MA; 1.7-3.0V)	PP2V6_CAM_AF
VLDO13	U17 (300MA; 1.7-3.0V)	PP2V9_CAM
ON_BUF	T10 (5MA; 1.8V; ON BUFF)	PP1V8_ALWAYS

VDD_LCM_SW	C17	=PPVCC_MAIN_VDD_LCM
VDD_BOOST_LCM	A18	PP6V0_LCM_HI (NOTE: 2MHZ)
BOOST_LCM_LX	B19	LCM_LX
LCM_FB	C15	
VDD_LCM	U11	PP6V0_LCM_VBOOST
VLCM1	V11 (100MA; 5.0-6.0V)	PP5V25_GRAPE
VLCM2	V12 (100MA; 5.0-6.0V) NO_TEST=TRUE	NC_VLCM2
LCM2_EN	E8	LCM2_EN
VLCM3	U12 (5MA; 5.0-6.0V) NO_TEST=TRUE	NC_VLCM3

- C8212 10UF 20% 25V X5R-CERM 0603
- C8210 2.2UF 20% 10V X5R-CERM 402
- CRITICAL C8211 10UF 20% 25V X5R-CERM 0402-2

CRITICAL L8229 2.2UH-1.05A-0.195OHM — WLS201612E-SM
MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, NET_SPACING_TYPE=PWR, DIDT=TRUE

CRITICAL D8230 PMEG2005AEL SOD882
VOLTAGE=6.0V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM

PMU_XTAL, PMU_EXTAL

CRITICAL Y8200 32.768K-20PPM-12.5PF 2012-1
- CRITICAL C8215 18PF 5% 25V C0G-CERM 0201
- CRITICAL C8216 18PF 5% 25V C0G-CERM 0201

R8250 1K 5% 1/20W MF 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392	?	Y8200	RDAR://PROBLEM/9936684

LDO BYPASS

PP3V0_SPARE1 — C8237 2.2UF 10% 6.3V X5R 402
PP1V7_VA_VCP — C8236 10UF 20% 6.3V CERM-X5R 0402
PP3V0_S2R_TRISTAR — C8235 4.7UF 20% 6.3V X5R-CERM 402
PP3V0_ALS — C8234 10UF 20% 6.3V CERM-X5R 0402
PP3V0_UVLO — C8233 2.2UF 10% 6.3V X5R 402
PP3V3_ACC — C8232 10UF 20% 6.3V CERM-X5R 0402
PP3V0_S2R_HALL — C8231 10UF 20% 6.3V CERM-X5R 0402
PP3V0_S2R_SENSOR — C8230 2.2UF 10% 6.3V X5R 402

PP1V3_CAM — C8242 0.22UF 10% 6.3V X5R 0201
PP1V0_SOC — C8241 10UF 20% 6.3V CERM-X5R 0402
PP2V6_CAM_AF — C8240 4.7UF 20% 6.3V X5R-CERM 402
PP2V9_CAM — C8239 4.7UF 20% 6.3V X5R-CERM 402
PP1V8_ALWAYS — C8238 4.7UF 20% 6.3V X5R-CERM 402

I2C ADDRESS: 0111100X (0X78)

OMIT_TABLE

U8100
D2089A0
FCBGA
SYM 3 OF 4

BUTTON1
BUTTON2
BUTTON3
BUTTON4
ACC_DET
ACC_ID
BRICK_ID
ADC_IN7
ADC_IN31
KEEPACT
SHDN
RESET_IN1
RESET_IN2
RESET_IN3
RESET*
IRQ*
SCL
SDA
DWI_CK
DWI_DI
DWI_DO
TDEV1
TDEV2
TDEV3
TDEV4
TDEV5
TDEV6
TDEV7
TDEV8
TBAT
TCAL
IREF
VREF
VDD_REF
VDD_REF_A
VDD_RTC
ADC_REF
OUT_32K
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
AMUX_A0
AMUX_A1
AMUX_A2
AMUX_A3
AMUX_AY
AMUX_B0
AMUX_B1
AMUX_B2
AMUX_B3
AMUX_BY

ANALOG INPUT
REFERENCES
DIGITAL INPUT
32K CLK
WDOG
RESET
GPIO
I2C & DWI
TEMPERATURE
ANALOG MUX

GPIO_BTN_HOME_L D5
GPIO_BTN_ONOFF_L D6
GPIO_BTN_SRL_L D7
GPIO_BTN_BUTTON4 D8
PMU_E75_ACC_DET_L T7
PMU_ACC_ID R12
PMU_USB_BRICKID_R P16
ADC_IN7 N16
R11
GPIO_SOC2PMU_KEEPACT T8
PMU_SHDWN (INTERNAL PULL-DOWN) T9
WDOG_SOC2PMU_RESET_IN (INTERNAL PULL-DOWN) R5
TS2PMU_RESET_IN R6
SOCHOT1_L R7
RESET_SOC_L R8
GPIO_PMU2SOC_IRQ_L (PULLUP INSIDE SOC) T15
I2C0_SCL_1V8 E12
I2C0_SDA_1V8 E13
DWI_AP_CLK (INTERNAL PULL-DOWN) E11
DWI_AP_DO (INTERNAL PULL-DOWN) E10
NC_DWI_AP_DI NO_TEST=TRUE E9
R9
R10
R13
R14
L4
M4
N4
P4
BATT_TNC R16
PMU_TCAL R15
PMU_IREF T12
PMU_VREF V13
PMU_VDD_REF M17
PMU_VDD_RTC U13
PMU_ADC_REF T13
PMU_OUT_32K_CLK_GPS T14
PMU_GPIO_CLK_32K_OSCAR T6
PMU_GPIO_CLK_32K_WLAN T5
PMU_GPIO_BT_REG_ON T4
PMU_GPIO_WLAN_REG_ON R3
PMU_GPIO_PMU2BBPMU_RST_R_L P3
UART5_BATT_TRXD N3
PMU_GPIO_BT_HOST_WAKE M3
PMU_GPIO_WLAN_HOST_WAKE L3
PMU_GPIO_BB2PMU_HOST_WAKE K3
PMU_GPIO_CODEC_HS_INT_L J3
PMU_GPIO_MB_HALL1_IRQ H3
GPIO_TS2SOC2PMU_INT G3
PMU_GPIO_MB_HALL2_IRQ F3
PMU_GPIO_CODEC_RST_L E3
NC_PMU_GPIO15 NO_TEST=TRUE D3
PMU_GPIO_OSCAR2PMU_HOST_WAKE C3
PMU_GPIO_BB_VBUS_DET C4
PPVDD_CPU_SOC_SENSE E4
PPVDD_GPU_SOC_SENSE F4
PPVDD_SOC_SENSE G6
TP_AMUX_A3 J6
TP_AMUX_AY G4
PPVDD_CPU_RAIL_SENSE K4
PPVDD_GPU_RAIL_SENSE J4
PPVDD_SOC_RAIL_SENSE K6
TP_AMUX_B3 L6
TP_AMUX_BY H4

R8398 0.00 5% 1/32W MF 01005
C8300 0.01UF 10% 6.3V X5R 01005
C8301 0.01UF 10% 6.3V X5R 01005
C8302 0.01UF 10% 6.3V X5R 01005
R8399 0 5% 1/20W MF 201
PMU_USB_BRICKID TRISTAR1 USE 6.34K
C8305 0.1UF 10% 6.3V CERM-X5R 0201
R8303 200K 1% 1/20W MF 201
C8306 0.1UF 10% 6.3V CERM-X5R 0201
C8307 1UF 10% 10V X5R 402-1
C8308 1.0UF 20% 10V X5R-CERM 0201-1
C8310 1000PF 10% 6.3V X5R-CERM 01005
R8330 1.00K 5% 1/32W MF 01005
PMU_GPIO_PMU2BBPMU_RST_L
C8340 100PF 5% 16V NP0-C0G 01005
R8340 3.92K 0.1% 0201 1/20W MF
RESISTOR FOR TEMP CALIBRATION

CRITICAL R8327 10KOHM-1%-0.31MA 0201 (TEMP1 - NEAR BB)
C8327 100PF 5% 16V NP0-C0G 01005
PA_NTC_P
PA_NTC_N

CRITICAL R8328 10KOHM-1%-0.31MA 0201 (TEMP2 - NEAR PROX)
C8328 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP2_P
BOARD_TEMP2_N

CRITICAL R8321 10KOHM-1%-0.31MA 0201 (TEMP3 - TOP SIDE NEAR WIFI)
C8321 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP3_P
BOARD_TEMP3_N

CRITICAL R8322 10KOHM-1%-0.31MA 0201 (TEMP4 - TOP SIDE NEAR AJ FLEX CONN)
C8322 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP4_P
BOARD_TEMP4_N

CRITICAL R8323 10KOHM-1%-0.31MA 0201 (TEMP5 - TOP SIDE NEAR NAND)
C8323 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP5_P
BOARD_TEMP5_N

CRITICAL R8324 10KOHM-1%-0.31MA 0201 (TEMP6 TOP SIDE NEAR REAR CAM)
C8324 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP6_P
BOARD_TEMP6_N

CRITICAL R8325 10KOHM-1%-0.31MA 0201 (TEMP7 - BOTTOM SIDE NEAR SOC)
C8325 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP7_P
BOARD_TEMP7_N

CRITICAL R8326 10KOHM-1%-0.31MA 0201 (TEMP8 - BOTTOM SIDE NEAR PMU)
C8326 100PF 5% 16V NP0-C0G 01005
BOARD_TEMP8_P
BOARD_TEMP8_N

PLACE XW AND CAP CLOSE TO PMU
XW8327 SM
XW8328 SM
XW8321 SM
XW8322 SM
XW8323 SM
XW8324 SM
XW8325 SM
XW8326 SM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8321,R8322,R8323,R8324,R8325,R8326

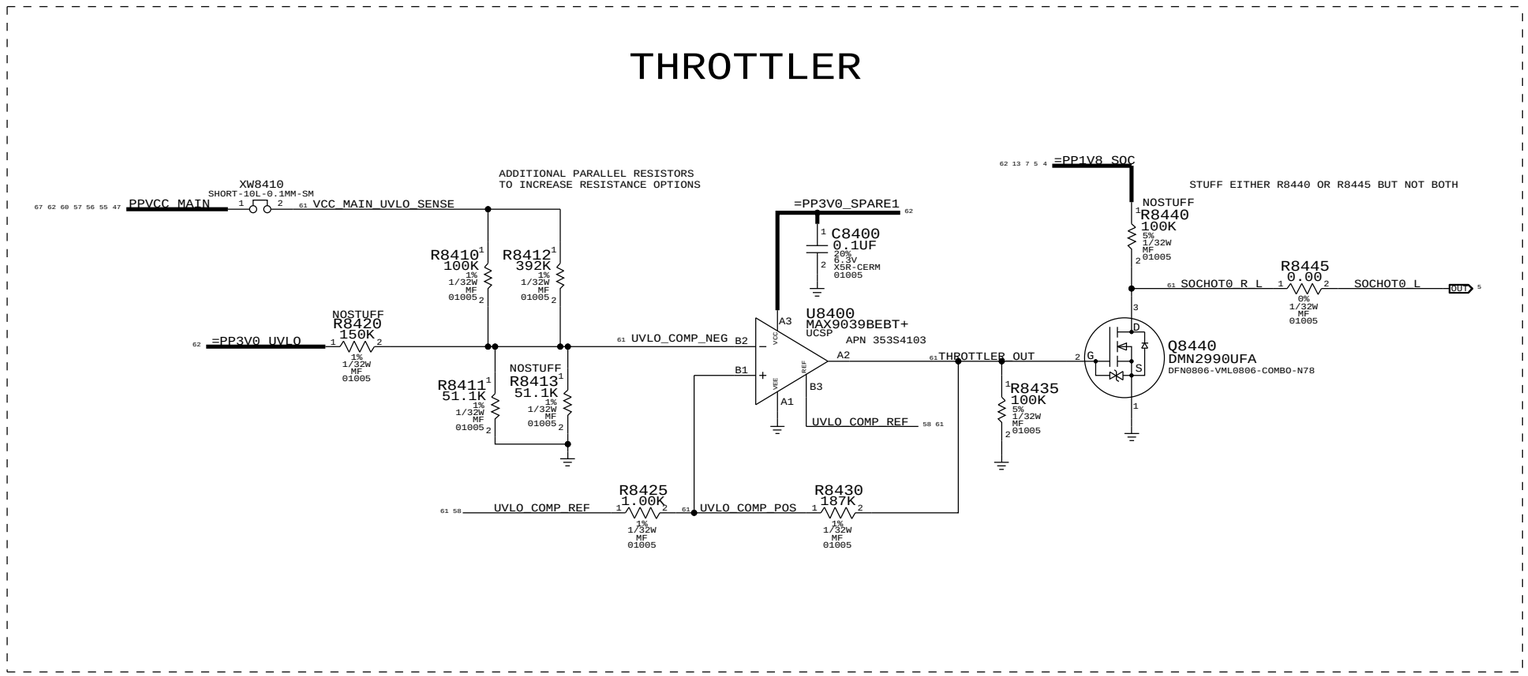
SWITCH TO GATE POWER TO SOC AND NAND. NEEDED FOR J72 ROUTING.

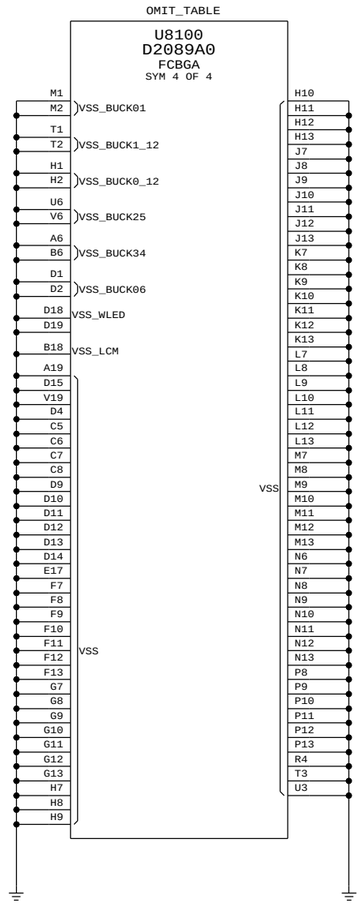
CRITICAL
U8360
TPS22924X
CSP
=PP1V8_S2R_EXT_SWITCH
PP1V8_EXT_SW
PP1V8_SW1
C8360 10UF 20% 10V X5R-CERM 0402-2
C8365 0.01UF 10% 6.3V X5R 01005

BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC

=PP3V3_S2R_SWITCH
PPVCC_MAIN
C8550 0.1UF 10% 16V X5R-CERM 0201
CRITICAL
U8350
SLG5AP1443V
TDFN
VDD
CAP
ON
GND
D
S
VCC_MAIN_PP3V3SW_RAMP
=PP1V8_NAND
PP3V3_SW
C8355 1.0UF 20% 6.3V X6S 0201-1
R8352 100K 5% 1/32W MF 01005
C8552 4700PF 10% 10V X7R 201
C8356 1.0UF 10% 10V X5R-CERM 0402-2

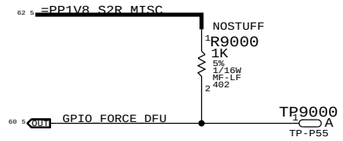
THROTTLER

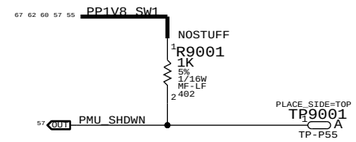




ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

DEBUG RESET ACCESS





SMT TEST FIXTURE TP

POWER

J211	PPVDD_CPU	FUNC_TEST=TRUE	55 62 67
J212	PPVDD_GPU	FUNC_TEST=TRUE	55 62 67
J213	PPVDD_SOC	FUNC_TEST=TRUE	55 62 67
J214	PP1V8_S2R	FUNC_TEST=TRUE	55 56 62 67
J215	PP1V8_SW1	FUNC_TEST=TRUE	55 57 59 62 67
J216	PP1V8_SW1_FOREHEAD	FUNC_TEST=TRUE	62 67
J217	PP1V8_EXT_SW	FUNC_TEST=TRUE	57 62 67
J218	PP1V8_SW2	FUNC_TEST=TRUE	55 62 67
J219	PP1V8_S2R_SW3	FUNC_TEST=TRUE	55 62 67
J220	PP1V8_S2R_SW3_COMP	FUNC_TEST=TRUE	62 67
J221	PP1V2_S2R	FUNC_TEST=TRUE	55 56 62 67
J222	PP1V2_SW1	FUNC_TEST=TRUE	55 62 67
J223	PP1V2_S2R_SW2	FUNC_TEST=TRUE	55 62 67
J224	PPVDD_SRAM	FUNC_TEST=TRUE	55 62 67
J225	PP3V3_S2R	FUNC_TEST=TRUE	55 62 67
J226	PP3V3_SW	FUNC_TEST=TRUE	57 62 67
J227	PP3V0_SPARE1	FUNC_TEST=TRUE	56 62 67
J228	PP1V7_VA_VCP	FUNC_TEST=TRUE	56 62 67
J229	PP3V0_S2R_SENSOR	FUNC_TEST=TRUE	56 62 67
J230	PP3V0_ALS	FUNC_TEST=TRUE	56 62 67
J231	PP3V3_ACC	FUNC_TEST=TRUE	56 62 67
J232	PP3V0_S2R_TRISTAR	FUNC_TEST=TRUE	56 62 67
J233	PP3V0_S2R_HALL	FUNC_TEST=TRUE	56 62 67
J234	PP1V3_CAM	FUNC_TEST=TRUE	56 62 67
J235	PP1V0_SOC	FUNC_TEST=TRUE	56 62 67
J236	PP2V6_CAM_AF	FUNC_TEST=TRUE	56 62 67
J237	PP2V9_CAM	FUNC_TEST=TRUE	56 62 67
J240	PP5V25_GRAPE	FUNC_TEST=TRUE	56 60 62 67
J241	PPVCC_MAIN	FUNC_TEST=TRUE	47 55 56 57 58 62 67
J242	PPBATT_VCC	FUNC_TEST=TRUE	55 60 62 67
J243	PPVBUS_USB_DCIN	FUNC_TEST=TRUE	55 62 67
J244	PP1V8_ALWAYS	FUNC_TEST=TRUE	56 62 67
J245	PPLED_OUT_A	FUNC_TEST=TRUE	56 62 67
J246	PPLED_OUT_B	FUNC_TEST=TRUE	56 62 67
J247	PP6V0_LCM_VBOOST	FUNC_TEST=TRUE	56 67

J402	PPBATT_POS_RC	FUNC_TEST=TRUE	55
J403	PMU_VCENTER	FUNC_TEST=TRUE	55 67
J404	PPVBUS_PROT	FUNC_TEST=TRUE	47 55 67
J407	VBUS_PROT_G	FUNC_TEST=TRUE	55

J290	PP1V2_CAM_FRONT_FILT	FUNC_TEST=TRUE	67
J291	PP1V3_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
J292	PP1V7_VCP	FUNC_TEST=TRUE	15 67
J295	PP1V8_CAM_FRONT_FILT	FUNC_TEST=TRUE	22 67
J296	PP1V8_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
J299	PP1V8_DMIC_FILT	FUNC_TEST=TRUE	16 67
J301	PP1V8_GRAPE_SW	FUNC_TEST=TRUE	51 52 61 67

J339	PP1V8_COMP	FUNC_TEST=TRUE	24 67
J340	PP2V6_CAM_REAR_AF_FILT	FUNC_TEST=TRUE	23 67
J341	PP2V9_AVDD_CAM_FRONT_FILT	FUNC_TEST=TRUE	22 67
J342	PP2V9_AVDD_CAM_REAR_FILT	FUNC_TEST=TRUE	23 67
J383	PP3V0_ALS_FILT	FUNC_TEST=TRUE	22 67
J384	PP3V0_HP_ALS_FILT	FUNC_TEST=TRUE	67
J385	PP3V0_IO_ALS_FILT	FUNC_TEST=TRUE	67
J386	PP3V0_S2R_HALL_FILT	FUNC_TEST=TRUE	20 50 67

J324	PP3V0_GYRO	FUNC_TEST=TRUE	19 67
J337	PP3V0_ACCEL	FUNC_TEST=TRUE	19 67
J336	PP3V0_COMP	FUNC_TEST=TRUE	24 67
J338	PP3V0_SENSOR_PROX_FILT	FUNC_TEST=TRUE	67
J388	PP3V0_SENSOR_PROX_ADUX1049_FILT	FUNC_TEST=TRUE	67
J381	PP3V0_SENSOR_PROX_AD7149_FILT	FUNC_TEST=TRUE	45 67
J382	PP5V25_GRAPE	FUNC_TEST=TRUE	56 60 62 67
J311	PPVCC_MAIN_LCD_SW_CONN	FUNC_TEST=TRUE	53 67
J345	PPVCC_MAIN_LCD_SW	FUNC_TEST=TRUE	53 67

J330	PP_SMPS1_MSMC_1V05	FUNC_TEST=TRUE	26 28 68
J327	PP_SMPS2_RF1_1V3	FUNC_TEST=TRUE	26 28 31 68
J331	PP_SMPS3_MSME_1V8	FUNC_TEST=TRUE	25 26 28 29 31
J328	PP_SMPS4_RF2_2V05	FUNC_TEST=TRUE	26 31 68
J335	PP_SMPS5_DSP_1V05	FUNC_TEST=TRUE	26 68

J284	PP_LDO1	FUNC_TEST=TRUE	26 68
T419	PP3V0_UVLO	FUNC_TEST=TRUE	56 62 67

J248	TP_BB_TEST_MODE_0	FUNC_TEST=TRUE	28
J241	TP_BB_TEST_MODE_1	FUNC_TEST=TRUE	28

T309	GPIO_SOC2OSCAR_DBGEN_R	FUNC_TEST=TRUE	19

TP9300	PPBATT_VCC	PLACE_NEAR=J7500.4:10MM	55 60 62 67
TP9301	PPBATT_VCC	PLACE_NEAR=J7500.4:10MM	55 60 62 67
TP9302	PPBATT_VCC	PLACE_NEAR=J7500.4:10MM	55 60 62 67
TP9305		PLACE_NEAR=J7500.3:10MM	
TP9306		PLACE_NEAR=J7500.3:10MM	
TP9307		PLACE_NEAR=J7500.3:10MM	
TP9310	PPVBUS_E75_USB_CONN	PLACE_NEAR=J6200.9:20MM	48 49 60 67
TP9311	PPVBUS_E75_USB_CONN	PLACE_NEAR=J6200.9:20MM	48 49 60 67
TP9312	PPVBUS_E75_USB_CONN	PLACE_NEAR=J6200.9:20MM	48 49 60 67
TP9315		PLACE_NEAR=TP9310.1:30MM	
TP9316		PLACE_NEAR=TP9310.1:30MM	
TP9317		PLACE_NEAR=TP9310.1:30MM	

All TP: A 1 TP-1P0-TOP

GPIO

J219	GPIO_CAM_ALS2SOC_IRQ_L_F	FUNC_TEST=TRUE	22
J220	GPIO_FORCE_DFU	FUNC_TEST=TRUE	5 59
J221	GPIO_GRAPE2SOC_IRQ_FILT_L	FUNC_TEST=TRUE	
J222	GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	5 25 27
J223	GPIO_SOC2BB_RST_L	FUNC_TEST=TRUE	5 25 27 67
J224	GPIO_SOC2GRAPE_RESET_FILT_L	FUNC_TEST=TRUE	5 52 61
J225	GPIO_OSCAR_RESET_L	FUNC_TEST=TRUE	5 19 67
J226	CLK_32K_SOC2CUMULUS_FILT	FUNC_TEST=TRUE	64
J227	HP_ALS_IRQ_L_CONN_FILT	FUNC_TEST=TRUE	

PMU GPIO

J228	PMU_GPIO_BB2PMU_HOST_WAKE	FUNC_TEST=TRUE	25 29 57
J229	PMU_GPIO_BT_REG_ON_R	FUNC_TEST=TRUE	46
J230	PMU_GPIO_CLK_32K_OSCAR	FUNC_TEST=TRUE	19 57 64
J231	PMU_GPIO_CLK_32K_WLAN_R	FUNC_TEST=TRUE	46
J232	PMU_GPIO_CODEC_HS_INT_L	FUNC_TEST=TRUE	15 57
J233	PMU_GPIO_PMU2BBPMU_RST_L	FUNC_TEST=TRUE	25 27 57 67
J234	PMU_GPIO_WLAN_REG_ON_R	FUNC_TEST=TRUE	46
J235	PMU_TCAL	FUNC_TEST=TRUE	57
J236	PMU_E75_ACC_DET_L	FUNC_TEST=TRUE	47 57
J237	TS_E75_ACC_DET_L	FUNC_TEST=TRUE	47
J238	PMU_GPIO_MB_HALL1_IRQ	FUNC_TEST=TRUE	20 57
J239	PMU_GPIO_MB_HALL2_IRQ	FUNC_TEST=TRUE	50 57

AUDIO

J243	CONN_HP_HEADSET_DET_FILT	FUNC_TEST=TRUE	15 16
J244	CONN_HP_HS3_FILT	FUNC_TEST=TRUE	15 16 60 65
J245	CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	15 16 60 65
J246	CONN_HP_HS3_FILT	FUNC_TEST=TRUE	15 16 60 65
J247	CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	15 16 60 65
J324	CONN_HP_HS4_FILT	FUNC_TEST=TRUE	15 16 65
J325	CONN_HP_HS4_REF_FILT	FUNC_TEST=TRUE	15 16 65
J326	CONN_HP_LEFT_FILT	FUNC_TEST=TRUE	15 16 65
J327	CONN_HP_RIGHT_FILT	FUNC_TEST=TRUE	15 16 65
J344	SPKRAMP_L1_OUT_N	FUNC_TEST=TRUE	18 49 65
J345	SPKRAMP_L1_OUT_P	FUNC_TEST=TRUE	18 49 65
J346	SPKRAMP_R1_OUT_N	FUNC_TEST=TRUE	17 49 65
J347	SPKRAMP_R1_OUT_P	FUNC_TEST=TRUE	17 49 65
J348	SPKRAMP_L2_OUT_N	FUNC_TEST=TRUE	18 49 65
J349	SPKRAMP_L2_OUT_P	FUNC_TEST=TRUE	18 49 65
J350	SPKRAMP_R2_OUT_N	FUNC_TEST=TRUE	17 49 65
J351	SPKRAMP_R2_OUT_P	FUNC_TEST=TRUE	17 49 65

J352	LEFT_CH_OUT_P	FUNC_TEST=TRUE	15 18 65
J353	LEFT_CH_OUT_N	FUNC_TEST=TRUE	15 18 65
J354	RIGHT_CH_OUT_P	FUNC_TEST=TRUE	15 17 65
J355	RIGHT_CH_OUT_N	FUNC_TEST=TRUE	15 17 65
J371	AIN3P	FUNC_TEST=TRUE	15
J372	AIN3N	FUNC_TEST=TRUE	15

J356	GND_AUDIO_CODEC	FUNC_TEST=TRUE	15 67
J357	DMIC1_FF_SCLK_FILT	FUNC_TEST=TRUE	16 64
J358	DMIC1_FF_SD_FILT	FUNC_TEST=TRUE	16 64
J414	L81_SPEAKER_VQ	FUNC_TEST=TRUE	15

GRAPE

J329	GPIO_GRAPE2SOC_IRQ_L	FUNC_TEST=TRUE	5 52 61
J330	GPIO_SOC2GRAPE_RESET_L	FUNC_TEST=TRUE	5 52 61 67
J331	CLK_32K_SOC2CUMULUS	FUNC_TEST=TRUE	5 52 61 64
J332	DISPLAY_SYNC	FUNC_TEST=TRUE	4 52 61
J333	SPI2_GRAPE_SCLK	FUNC_TEST=TRUE	5 52 61 64
J334	SPI2_GRAPE_MISO	FUNC_TEST=TRUE	5 52 61 64
J335	SPI2_GRAPE_MOSI	FUNC_TEST=TRUE	5 52 61 64
J336	SPI2_GRAPE_CS_L	FUNC_TEST=TRUE	5 52 61 64
J337	VCC_MAIN_GRAPE_RAMP	FUNC_TEST=TRUE	51

UART

J360	UART0_SOC_RXD	FUNC_TEST=TRUE	5 47 64
J361	UART0_SOC_TXD	FUNC_TEST=TRUE	5 47 64

TEST POINT RULES:
CENTER TO CENTER SPACING >= 1MM
DIAMETER >= 0.5MM
EDGE TO SHIELD >=0.55MM

BACKLIGHT

J48	PPLED_BACK_REG_A	FUNC_TEST=TRUE	53 67
J49	LED_IO_1_A	FUNC_TEST=TRUE	53 56 65
J50	LED_IO_2_A	FUNC_TEST=TRUE	53 56 65
J51	LED_IO_3_A	FUNC_TEST=TRUE	53 56 65
J52	LED_IO_4_A	FUNC_TEST=TRUE	53 56 65
J53	LED_IO_5_A	FUNC_TEST=TRUE	53 56 65
J54	LED_IO_6_A	FUNC_TEST=TRUE	53 56 65
J55	PPLED_BACK_REG_B	FUNC_TEST=TRUE	53 67
J56	LED_IO_1_B	FUNC_TEST=TRUE	53 56 65
J57	LED_IO_2_B	FUNC_TEST=TRUE	53 56 65
J58	LED_IO_3_B	FUNC_TEST=TRUE	53 56 65
J59	LED_IO_4_B	FUNC_TEST=TRUE	53 56 65
J67	LED_IO_5_B	FUNC_TEST=TRUE	53 56 65
J68	LED_IO_6_B	FUNC_TEST=TRUE	53 56 65

BATTERY

J63	BATT_SWI_CONN	FUNC_TEST=TRUE	54 64
J64	BATT_NTC	FUNC_TEST=TRUE	54 57 60 67

E75

J65	E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	47 49 60
J66	PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	48 49 60 67
J67	PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	48 49 60 67
J68	E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	47 49 60 64
J69	E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	47 49 60 64
J70	E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	47 49 60 64
J71	E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	47 49 60 64
J72	PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	48 49 60 67

REEST JTAG/CONFIG

J73	JTAG_SOC_SEL	FUNC_TEST=TRUE	4 13
J74	JTAG_SOC_TCK	FUNC_TEST=TRUE	4 47 64
J75	JTAG_SOC_TDI	FUNC_TEST=TRUE	4 64
J76	TP_JTAG_SOC_TDO	FUNC_TEST=TRUE	4 64
J77	JTAG_SOC_TMS	FUNC_TEST=TRUE	4 47 64
J78	JTAG_SOC_TRST_L	FUNC_TEST=TRUE	4 13 64
J77	SOC_TESTMODE	FUNC_TEST=TRUE	4 13
J200	RESET_SOC_L	FUNC_TEST=TRUE	4 13 25 47 57 61 67
J310	PS_HOLD_PMIC	FUNC_TEST=TRUE	25 27

BUTTONS

J424	GPIO_BTN_ONOFF_L_FILT	FUNC_TEST=TRUE	21
J425	GPIO_BTN_HOME_L	FUNC_TEST=TRUE	5 59 57
J426	GPIO_BTN_VOL_UP_L_FILT	FUNC_TEST=TRUE	21
J427	GPIO_BTN_VOL_DOWN_L_FILT	FUNC_TEST=TRUE	21
J428	GPIO_BTN_SRL_L_FILT	FUNC_TEST=TRUE	21

BOARD TEMP

J455	PA_NTC_P	FUNC_TEST=TRUE	57 65
J446	BOARD_TEMP2_P	FUNC_TEST=TRUE	57 65
J447	BOARD_TEMP3_P	FUNC_TEST=TRUE	57 65
J448	BOARD_TEMP4_P	FUNC_TEST=TRUE	57 65
J449	BOARD_TEMP5_P	FUNC_TEST=TRUE	57 65
J450	BOARD_TEMP6_P	FUNC_TEST=TRUE	57 65
J451	BOARD_TEMP7_P	FUNC_TEST=TRUE	57 65
J452	BOARD_TEMP8_P	FUNC_TEST=TRUE	57 65

USB

J408	USB_SOC_N	FUNC_TEST=TRUE	4 47 64
J409	USB_SOC_P	FUNC_TEST=TRUE	4 47 64

CAMERA

J430	ISP0_CAM_REAR_CLK_F	FUNC_TEST=TRUE	23 64
J431	ISP0_CAM_REAR_SCL_F	FUNC_TEST=TRUE	23 64
J432	ISP0_CAM_REAR_SDA_F	FUNC_TEST=TRUE	23 64
J433	ISP0_CAM_REAR_SHUTDOWN_L_F	FUNC_TEST=TRUE	23 67
J434	ISP1_CAM_FRONT_CLK_F	FUNC_TEST=TRUE	22 64
J435	ISP1_CAM_FRONT_SCL_F	FUNC_TEST=TRUE	22 64
J436	ISP1_CAM_FRONT_SDA_F	FUNC_TEST=TRUE	22 64
J437	ISP1_CAM_FRONT_SHUTDOWN_L_F	FUNC_TEST=TRUE	22 67

NAND

J472	FMI0_CE0_L	FUNC_TEST=TRUE	6 14 61 66

DISPLAY

J313	DISPLAY_SYNC_FILT	FUNC_TEST=TRUE	

I2C

J453	I2C3_CAM_ALS_SCL_1V8_F	FUNC_TEST=TRUE	22 64
J454	I2C3_CAM_ALS_SDA_1V8_F	FUNC_TEST=TRUE	22 64
J455	I2C0_HP_ALS_SCL_1V8_FILT	FUNC_TEST=TRUE	64
J456	I2C0_HP_ALS_SDA_1V8_FILT	FUNC_TEST=TRUE	64
J426	I2C0_SCL_1V8	FUNC_TEST=TRUE	5 57 64
J425	I2C0_SDA_1V8	FUNC_TEST=TRUE	5 57 64

SIM

J470	SIMCRD_RST_CONN	FUNC_TEST=TRUE	29 44
J471	SIMCRD_CLK_CONN	FUNC_TEST=TRUE	29 44
J472	SIMCRD_IO_CONN	FUNC_TEST=TRUE	29 44
J473	SIM_TRAY_DETECT	FUNC_TEST=TRUE	29 44
J474	PP_LDO6_RUIM_1V8	FUNC_TEST=TRUE	26 28 44 68

RF FIXTURE

J314	E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	47 49 60 64
J315	E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	47 49 60 64
J316	E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	47 49 60 64
J317	E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	47 49 60 64
J405	PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	48 49 60 67
J406	PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	48 49 60 67
J407	PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	48 49 60 67
J408	E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	47 49 60
J409	BATT_NTC	FUNC_TEST=TRUE	54 57 60 67

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9310 TH-NSP 1 SL-1.1X0.4-1.4X0.7
SL9311 TH-NSP 1 SL-1.1X0.4-1.4X0.7

FOREHEAD B2B STANDOFFS

STD9300 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9301 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9302 STDOFF-3.3X1.8R1.02H-SM 1 NOTE: BOTTOM OF FOREHEAD

GRAPE AND DISPLAY B2B STANDOFFS

STD9305 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9306 STDOFF-3.3X1.8R1.17H-SM-1 1
STD9307 STDOFF-3.3X1.8R1.17H-SM-1 1

FID9300 FID 0P5SM1P0SQ-NSP 1
FID9301 FID 0P5SM1P0SQ-NSP 1
FID9302 FID 0P5SM1P0SQ-NSP 1
FID9303 FID 0P5SM1P0SQ-NSP 1
FID9304 FID 0P5SM1P0SQ-NSP 1
FID9305 FID 0P5SM1P0SQ-NSP 1

EE CHARACTERIZATION TP

NAND

BOTTOM SIDE PP9460 P4MM SM (PP) 1 FMI0_AD<0> PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.A32:2MM NO_XNET_CONNECTION=TRUE 6 14 61 66
BOTTOM SIDE PP9461 P4MM SM (PP) 1 FMI0_DQS PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.B34:2MM NO_XNET_CONNECTION=TRUE 6 14 61 66

FMI0_AD<0..7> EE_TEST=TRUE FUNC_TEST=TRUE 6 14 61 66
FMI0_CE0_L FUNC_TEST=TRUE 6 14 60 66
FMI0_ALE FUNC_TEST=TRUE 6 14 66
FMI0_CLE FUNC_TEST=TRUE 6 14 66
FMI0_WE_L FUNC_TEST=TRUE 6 14 66
FMI0_RE_L FUNC_TEST=TRUE 6 14 66
FMI0_DQS FUNC_TEST=TRUE 6 14 61 66

FMI1_AD<0> FUNC_TEST=TRUE 6 14 66
FMI1_CE0_L 6 14 66
FMI1_ALE 6 14 66
FMI1_CLE 6 14 66
FMI1_WE_L 6 14 66
FMI1_RE_L 6 14 66
FMI1_DQS 6 14 66

PPVREF_FMI_SOC FUNC_TEST=TRUE 6 66
PPVREF_FMI_NAND FUNC_TEST=TRUE 14 66

TOP SIDE PP9440 P4MM SM (PP) 1 TP_FMI_TCKC_NAND PLACE_SIDE=TOP 14
TOP SIDE PP9441 P4MM SM (PP) 1 TP_FMI_TMSC_NAND PLACE_SIDE=TOP 14
TOP SIDE PP9442 P4MM SM (PP) 1 =PP1V8_NAND PLACE_SIDE=TOP 14 57 62
TOP SIDE PP9443 P4MM SM (PP) 1 GND PLACE_SIDE=TOP

EE

TOP SIDE PP9450 P4MM SM (PP) 1 RESET_SOC_L 4 13 25 47 57 60 67
PP9451 P4MM SM (PP) 1 TP_ANALOGMUXOUT 4
TOP SIDE PP9452 P4MM SM (PP) 1 SOCHOT0_R_L 58

TP_GPIO_DFU_STATUS FUNC_TEST=TRUE 5

CAMERA

PP9470 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_P PLACE_NEAR=U0600.AM35:3MM NO_XNET_CONNECTION=TRUE 7 22 61 65
PP9471 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_N PLACE_NEAR=U0600.AM36:3MM NO_XNET_CONNECTION=TRUE 7 22 61 65
PP9472 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_P<0> PLACE_NEAR=U0600.AN35:3MM NO_XNET_CONNECTION=TRUE 7 22 61 65
PP9473 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_N<0> PLACE_NEAR=U0600.AN36:3MM NO_XNET_CONNECTION=TRUE 7 22 61 65
PP9474 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_P PLACE_NEAR=U0600.AR31:3MM NO_XNET_CONNECTION=TRUE 7 23 61 65
PP9475 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_N PLACE_NEAR=U0600.AT31:3MM NO_XNET_CONNECTION=TRUE 7 23 61 65
PP9476 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_P<0> PLACE_NEAR=U0600.AR33:3MM NO_XNET_CONNECTION=TRUE 7 23 61 65
PP9477 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_N<0> PLACE_NEAR=U0600.AT33:3MM NO_XNET_CONNECTION=TRUE 7 23 61 65

FOR FRANK (SEG)

PP9400 P4MM SM (PP) 1 PPVDD_SOC_SOC_SENSE PLACE_NEAR=U0600.V31:1MM 10 57 67
PP9401 P4MM SM (PP) 1 PPVDD_CPU_SOC_SENSE PLACE_NEAR=U0600.AL31:1MM 11 57 67
PP9402 P4MM SM (PP) 1 PPVDD_GPU_SOC_SENSE PLACE_NEAR=U0600.AA7:1MM 11 57 67

DRAM

NEAR DRAM

PP9410 P4MM SM (PP) 1 DDR0_CK_N PLACE_NEAR=U1400.AF14:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9411 P4MM SM (PP) 1 DDR0_CK_P PLACE_NEAR=U1400.AF15:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9412 P4MM SM (PP) 1 DDR0_CKE<0> PLACE_NEAR=U1400.AF16:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9413 P4MM SM (PP) 1 DDR0_CKE<1> PLACE_NEAR=U1400.AE17:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9414 P4MM SM (PP) 1 DDR0_CA<0> PLACE_NEAR=U1400.AE21:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9415 P4MM SM (PP) 1 DDR0_DQ<2> PLACE_NEAR=U1400.B18:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9416 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U1400.C8:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9417 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U1400.B8:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9418 P4MM SM (PP) 1 DDR0_DQS_N<0> PLACE_NEAR=U1400.C15:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9419 P4MM SM (PP) 1 DDR0_DQS_P<0> PLACE_NEAR=U1400.B15:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66

PP9420 P4MM SM (PP) 1 DDR1_CK_N PLACE_NEAR=U1400.T26:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9421 P4MM SM (PP) 1 DDR1_CK_P PLACE_NEAR=U1400.R26:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9422 P4MM SM (PP) 1 DDR1_CKE<0> PLACE_NEAR=U1400.P26:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9423 P4MM SM (PP) 1 DDR1_CKE<1> PLACE_NEAR=U1400.N25:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9424 P4MM SM (PP) 1 DDR1_CA<0> PLACE_NEAR=U1400.J25:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9425 P4MM SM (PP) 1 DDR1_CA<1> PLACE_NEAR=U1400.K26:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9426 P4MM SM (PP) 1 DDR1_CA<2> PLACE_NEAR=U1400.K25:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9427 P4MM SM (PP) 1 DDR1_CA<3> PLACE_NEAR=U1400.L25:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9428 P4MM SM (PP) 1 DDR1_CSN<0> PLACE_NEAR=U1400.N35:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66

NEAR SOC

PP9435 P4MM SM (PP) 1 DDR0_DQ<28> PLACE_NEAR=U0600.D5:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9436 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U0600.A6:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66
PP9437 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U0600.A5:1MM NO_XNET_CONNECTION=TRUE 8 12 61 66

GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

TP_JTAG_CUMULUS_M_TCK 52 64
TP_JTAG_CUMULUS_M_TDI 52 64
JTAG_CUMULUS_M_TMS 52 64
TP_JTAG_CUMULUS_M_TDO 52 64
DISPLAY_SYNC 4 52 60
CUMULUS_MS_CK 52 64
CUMULUS_MS_SD 52 64

GPIO_GRAPE2SOC_IRQ_L 5 52 60
GPIO_SOC2GRAPE_RESET_L 5 52 60 67
CLK_32K_SOC2CUMULUS 5 52 60 64
SPI2_GRAPE_MOSI 5 52 60 64
SPI2_GRAPE_MISO 5 52 60 64
SPI2_GRAPE_SCLK 5 52 60 64
SPI2_GRAPE_CS_L 5 52 60 64
TP_CUMULUS_S_H_CS_L 52
TP_CUMULUS_S_H_SCLK 52
TP_CUMULUS_S_H_SDI 52
TP_CUMULUS_S_H_SDO 52

=PP5V25_GRAPE 52 62
PP1V8_GRAPE_SW 51 52 60 67

GRAPE NO_TEST

MT_PANEL_IN<0..29> NO_TEST=TRUE 52 65
MT_PANEL_OUT<0..39> NO_TEST=TRUE 52 65

AUDIO

L81_DMIC1_FF_SD FUNC_TEST=TRUE 15

WIFI

JTAG_WLAN_TMS_TX_BLANK FUNC_TEST=TRUE 46 64
TP_JTAG_WLAN_TCK FUNC_TEST=TRUE 46 64
JTAG_WLAN_TDI_OSCAR_A FUNC_TEST=TRUE 46 64
JTAG_WLAN_TDO_OSCAR_B FUNC_TEST=TRUE 46 64
TP_JTAG_WLAN_TRST_L FUNC_TEST=TRUE 46 64
JTAG_WLAN_SEL FUNC_TEST=TRUE 46
UART2_SOC2WLAN_TX_R FUNC_TEST=TRUE 46 64
UART2_WLAN2SOC_TX_R FUNC_TEST=TRUE 46 64
UART_BB2WLAN_LTE_COEX_R FUNC_TEST=TRUE 46
UART_WLAN2BB_LTE_COEX_R FUNC_TEST=TRUE 46
=PP3V3_S2R_WIFI_PA FUNC_TEST=TRUE 46 62

HSIC1_SOC2WLAN_HOST_RDY_R FUNC_TEST=TRUE 46 64
HSIC1_WLAN2SOC_DEVICE_RDY FUNC_TEST=TRUE 5 46 64
HSIC1_WLAN2SOC_REMOTE_WAKE FUNC_TEST=TRUE 5 46 64

FOR HSIC CHARACTERIZATION

PP9480 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U0600.A27:3MM 4 46 61 64
PP9481 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U0600.B27:3MM 4 46 61 64
PP9482 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U5800.13:3MM 4 46 61 64
PP9483 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U5800.14:3MM 4 46 61 64

PMU_GPIO_WLAN_REG_ON FUNC_TEST=TRUE 46 57
PMU_GPIO_BT_REG_ON FUNC_TEST=TRUE 46 57
GPIO_BT_WAKE FUNC_TEST=TRUE 5 46

BASEBAND

BB_JTAG_TMS FUNC_TEST=TRUE 5 25 28 64
BB_JTAG_TCK FUNC_TEST=TRUE 5 25 28 64
BB_JTAG_TDI FUNC_TEST=TRUE 5 25 28 64
BB_JTAG_TDO FUNC_TEST=TRUE 5 25 28 64
BB_JTAG_TRST_L FUNC_TEST=TRUE 5 25 28 64
USB_BB_DEBUG_P FUNC_TEST=TRUE 25 28 64
USB_BB_DEBUG_N FUNC_TEST=TRUE 25 28 64
DEBUG_RST_L FUNC_TEST=TRUE 25 28 67
PMU_GPIO_BB_VBUS_DET FUNC_TEST=TRUE 25 28 57 67

FOR HSIC CHARACTERIZATION

PP9485 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U0600.AJ35:3MM 4 25 28 61 64
PP9486 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U0600.AJ36:3MM 4 25 28 61 64
PP9487 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U3400.C7:3MM 4 25 28 61 64
PP9488 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U3400.B8:3MM 4 25 28 61 64

HIGH SPEED, NO TEST

DDR0_CA<0..9> NO_TEST=TRUE 8 12 61 66
DDR0_CK_P NO_TEST=TRUE 8 12 61 66
DDR0_CK_N NO_TEST=TRUE 8 12 61 66
DDR0_CA<0..9> NO_TEST=TRUE 8 12 61 66
DDR0_CKE<0..1> NO_TEST=TRUE 8 12 61 66
DDR0_CSN<0..1> NO_TEST=TRUE 8 12 66
DDR0_DM<0..3> NO_TEST=TRUE 8 12 66
DDR0_DQ<0..31> NO_TEST=TRUE 8 12 61 66
DDR0_DQS_P<0..3> NO_TEST=TRUE 8 12 61 66
DDR0_DQS_N<0..3> NO_TEST=TRUE 8 12 61 66

DDR1_CA<0..9> NO_TEST=TRUE 8 12 61 66
DDR1_CK_P NO_TEST=TRUE 8 12 61 66
DDR1_CK_N NO_TEST=TRUE 8 12 61 66
DDR1_CA<0..9> NO_TEST=TRUE 8 12 61 66
DDR1_CKE<0..1> NO_TEST=TRUE 8 12 61 66
DDR1_CSN<0..1> NO_TEST=TRUE 8 12 61 66
DDR1_DM<0..3> NO_TEST=TRUE 8 12 66
DDR1_DQ<0..31> NO_TEST=TRUE 8 12 66
DDR1_DQS_P<0..3> NO_TEST=TRUE 8 12 66
DDR1_DQS_N<0..3> NO_TEST=TRUE 8 12 66

MIPI0C_CAM_REAR_CLK_P NO_TEST=TRUE 7 23 61 65
MIPI0C_CAM_REAR_CLK_N NO_TEST=TRUE 7 23 61 65
MIPI0C_CAM_REAR_DATA_P<0..1> NO_TEST=TRUE 7 23 61 65
MIPI0C_CAM_REAR_DATA_N<0..1> NO_TEST=TRUE 7 23 61 65
MIPI0C_CAM_REAR_CLK_FILT_P NO_TEST=TRUE 23 65
MIPI0C_CAM_REAR_CLK_FILT_N NO_TEST=TRUE 23 65
MIPI0C_CAM_REAR_DATA_FILT_P<0..3> NO_TEST=TRUE 23 65
MIPI0C_CAM_REAR_DATA_FILT_N<0..3> NO_TEST=TRUE 23 65
MIPI1C_CAM_FRONT_CLK_P NO_TEST=TRUE 7 22 61 65
MIPI1C_CAM_FRONT_CLK_N NO_TEST=TRUE 7 22 61 65
MIPI1C_CAM_FRONT_DATA_P<0> NO_TEST=TRUE 7 22 61 65
MIPI1C_CAM_FRONT_DATA_N<0> NO_TEST=TRUE 7 22 61 65
MIPI1C_CAM_FRONT_CLK_FILT_P NO_TEST=TRUE 22 65
MIPI1C_CAM_FRONT_CLK_FILT_N NO_TEST=TRUE 22 65
MIPI1C_CAM_FRONT_DATA_FILT_P<0> NO_TEST=TRUE 22 65
MIPI1C_CAM_FRONT_DATA_FILT_N<0> NO_TEST=TRUE 22 65

EDP_DATA_P<0..3> NO_TEST=TRUE 7 53 65
EDP_DATA_N<0..3> NO_TEST=TRUE 7 53 65
EDP_DATA_EMI_P<0..3> NO_TEST=TRUE 53 65
EDP_DATA_EMI_N<0..3> NO_TEST=TRUE 53 65
EDP_DATA_EMI_CONN_P<0..3> NO_TEST=TRUE 53 65
EDP_DATA_EMI_CONN_N<0..3> NO_TEST=TRUE 53 65

POWER, NO TEST

PP6V0_LCM_HI NO_TEST=TRUE 56 67
SW_CHGA NO_TEST=TRUE 55 67
WLED_LX_A NO_TEST=TRUE 56 67
WLED_LX_B NO_TEST=TRUE 56 67

L81_PVCP NO_TEST=TRUE 15 65
L81_NVCP NO_TEST=TRUE 15 65

CHARGE PUMP OUTPUTS

L81_FLYC NO_TEST=TRUE 15 65
L81_FLYN NO_TEST=TRUE 15 65
L81_FLYP NO_TEST=TRUE 15 65

THROTTLER_OUT NO_TEST=TRUE 58
UVLO_COMP_NEG NO_TEST=TRUE 58
UVLO_COMP_POS NO_TEST=TRUE 58
UVLO_COMP_REF NO_TEST=TRUE 58
VCC_MAIN_UVLO_SENSE NO_TEST=TRUE 58

NO TEST DUE TO LAYOUT

I2C3 TP AT ALS FILTER SIDE

I2C3_SCL_1V8 NO_TEST=TRUE 5 13 22 64
I2C3_SDA_1V8 NO_TEST=TRUE 5 13 22 64

MAX98304_L1_IN_N NO_TEST=TRUE 18 65
MAX98304_L1_IN_P NO_TEST=TRUE 18 65
MAX98304_R1_IN_N NO_TEST=TRUE 17 65
MAX98304_R1_IN_P NO_TEST=TRUE 17 65
MAX98304_L2_IN_N NO_TEST=TRUE 18 65
MAX98304_L2_IN_P NO_TEST=TRUE 18 65
MAX98304_R2_IN_N NO_TEST=TRUE 17 65
MAX98304_R2_IN_P NO_TEST=TRUE 17 65

GPIO_BTN_HOME_CONN_R_L NO_TEST=TRUE 50

NO TEST ON PROX

PROX_AD7149_CIN5 NO_TEST=TRUE 45
PROX_AD7149_CIN7 NO_TEST=TRUE 45
PROX_AD7149_CIN9 NO_TEST=TRUE 45
PROX_AD7149_CIN7_FILT NO_TEST=TRUE 45
PROX_AD7149_CIN9_FILT NO_TEST=TRUE 45
PROX_AD7149_CIN7_CONN NO_TEST=TRUE 45
PROX_AD7149_CIN9_CONN NO_TEST=TRUE 45
PROX_AD7149_ACSHIELD_CONN NO_TEST=TRUE 45
PROX_AD7149_BIAS NO_TEST=TRUE 45
ACSHIELD_SB NO_TEST=TRUE 45
ACSH_SB NO_TEST=TRUE 45
PROX_AD7149_GPIO NO_TEST=TRUE 45

POWER CONNECTIONS

BUCK0

67 60 55 PPVDD_CPU (MAKE_BASE=TRUE) = =PPVDD_CPU 11

BUCK1

67 60 55 PPVDD_GPU (MAKE_BASE=TRUE) = =PPVDD_GPU 11

BUCK2

67 60 55 PPVDD_SOC (MAKE_BASE=TRUE) = =PPVDD_SOC 10

BUCK3

67 60 56 55 PP1V8_S2R (MAKE_BASE=TRUE)
- = =PP1V8_S2R_MISC 5 59
- = =PP1V8_S2R_VDDIO_WLAN_BT 46
- = =PP1V8_S2R_TRISTAR 47
- = =PP1V8_S2R_DDR 12
- = =PP1V8_S2R_GRAPE 51
- = =PP1V8_S2R_EXT_SWITCH 57

BUCK3_SW

67 60 59 57 55 PP1V8_SW1 (MAKE_BASE=TRUE) = =PP1V8_AUDIO 15

XWC130 SM 1 2 PP1V8_SW1_FOREHEAD 60 62 67

67 62 60 PP1V8_SW1_FOREHEAD (MAKE_BASE=TRUE)
- = =PP1V8_DMIC 16
- = =PP1V8_CAM_FRONT 22
- = =PP1V8_CAM_REAR 23
- = =PP1V8_PROX_AD7149 45

67 60 57 PP1V8_EXT_SW (MAKE_BASE=TRUE)
- = =PP1V8_VDDIO18_SOC 9 10
- = =PP1V8_SOC 4 5 7 13 58
- = =PP1V8_MIPI_SOC 7
- = =PP1V8_EDP_SOC 7
- = =PP1V8_NAND_SOC 6
- = =PP1V8_NAND 14 57 61
- = =PP1V8_PLL_SOC 4
- = =PP1V8_EEPROM 5

67 60 55 PP1V8_SW2 (MAKE_BASE=TRUE) = =PP1V8_GRAPE 51

67 60 55 PP1V8_S2R_SW3 (MAKE_BASE=TRUE)
- = =PP1V8_S2R_GYRO 19
- = =PP1V8_S2R_ACCEL 19
- = =PP1V8_S2R_OSCAR 19

XWC133 SM 1 2 PP1V8_S2R_SW3_COMP 60 62 67

67 62 60 PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) = =PP1V8_S2R_COMP 24

BUCK4

67 60 56 55 PP1V2_S2R (MAKE_BASE=TRUE)
- = =PP1V2_S2R_DDR 12
- = =PP1V2_S2R_DDR_SOC 8

BUCK4_SW

67 60 55 PP1V2_SW1 (MAKE_BASE=TRUE)
- = =PP1V2_VDDQ_DDR 12
- = =PP1V2_VDDIOD_SOC 8 9
- = =PP1V2_HSIC_SOC 4

67 60 55 PP1V2_S2R_SW2 (MAKE_BASE=TRUE) = =PP1V2_S2R_OSCAR 19

BUCK5

67 60 55 PPVDD_SRAM (MAKE_BASE=TRUE)
- = =PPVDD_SRAM_CPU 10
- = =PPVDD_SRAM_SOC 10

BUCK6

67 60 55 PP3V3_S2R (MAKE_BASE=TRUE)
- = =PP3V3_S2R_SWITCH 57
- = =PP3V3_S2R_WIFI_PA 46 61

67 60 57 PP3V3_SW (MAKE_BASE=TRUE)
- = =PP3V3_EDP_PU
- = =PP3V3_NAND 14
- = =PP3V3_USB_SOC 4

LDO1

67 60 56 PP3V0_SPARE1 (MAKE_BASE=TRUE) = =PP3V0_SPARE1 58

LDO2

67 60 56 PP1V7_VA_VCP (MAKE_BASE=TRUE) = =PP1V7_VA_VCP 15

LDO3

67 60 56 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE)
- = =PP3V0_S2R_GYRO 19
- = =PP3V0_S2R_ACCEL 19
- = =PP3V0_S2R_COMP 24

LDO4

67 60 56 PP3V0_ALS (MAKE_BASE=TRUE)
- = =PP3V0_ALS 22
- = =PP3V0_PROX_AD7149 45

LDO5

67 60 56 PP3V0_UVLO (MAKE_BASE=TRUE) = =PP3V0_UVLO 58

LDO6

67 60 56 PP3V3_ACC (MAKE_BASE=TRUE) = =PP3V3_ACC 47

LDO7

67 60 56 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) = =PP3V0_S2R_TRISTAR 47

LDO8

67 60 56 PP3V0_S2R_HALL (MAKE_BASE=TRUE) = =PP3V0_S2R_HALL 50

LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET 1.1V MIN ON CAMERA IF NEEDED.

67 60 56 PP1V3_CAM (MAKE_BASE=TRUE) = =PP1V3_CAM_REAR 23

LDO10

67 60 56 PP1V0_SOC (MAKE_BASE=TRUE)
- = =PP1V0_USB_SOC 4
- = =PP1V0_MIPI_SOC 7
- = =PP1V0_EDP_PAD_DVDD_SOC 7

LDO011

67 60 56 PP2V6_CAM_AF (MAKE_BASE=TRUE) = =PP2V6_CAM_REAR_AF 23

LDO013

67 60 56 PP2V9_CAM (MAKE_BASE=TRUE)
- = =PP2V9_CAM_FRONT 22
- = =PP2V9_CAM_REAR 23

VLCM1

67 60 56 PP5V25_GRAPE (MAKE_BASE=TRUE) = =PP5V25_GRAPE 52 61

CHARGER MAIN

67 60 58 57 56 55 47 PPVCC_MAIN (MAKE_BASE=TRUE)
- = =PPVCC_MAIN_AUDIO 15
- = =PPVCC_MAIN_LED 56
- = =PPVCC_MAIN_CPU 55
- = =PPVCC_MAIN_GPU 55
- = =PPVCC_MAIN_SOC 55
- = =PPVCC_MAIN_GRAPE 51
- = =PPVCC_MAIN_LCD 53
- = =PPVCC_MAIN_VDD_LCM 56
- = =PPVCC_MAIN_WLAN 46

BATTERY

67 60 55 PPBATT_VCC (MAKE_BASE=TRUE)
- = =PPBATT_POS_CONN 54
- = =PPBATT_VCC_BB 25 26 34 35 36 37 38 39 40
- = =PPBATT_AUDIO 17 18

USB POWER INPUT

67 60 55 PPVBUS_USB_DCIN (MAKE_BASE=TRUE) = =PPVBUS_USB_EMI 48

ON_BUF

67 60 56 PP1V8_ALWAYS (MAKE_BASE=TRUE) = =PP1V8_ALWAYS 5

BACKLIGHT BOOST

67 60 56 PPLED_OUT_A (MAKE_BASE=TRUE) = =PPLED_REG_A 53

67 60 56 PPLED_OUT_B (MAKE_BASE=TRUE) = =PPLED_REG_B 53

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B6	CLK_50S	CLK	CLK_32K_SOC2CUMULUS 5 52 60 61
B5	CLK_50S	CLK	CLK_32K_SOC2CUMULUS_FILT 60
B4	CLK_50S	CLK	CUMULUS_MS_CK 52 61
B3	CLK_50S	CLK	CUMULUS_MS_SD 52 61
B2	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 46 57
B1	CLK_50S	CLK	PMU_GPIO_CLK_32K_OSCAR 19 57 60
A1	CLK_50S	CLK	PMU_OUT_32K_CLK_GPS 57 68
B8	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_R 7
B7	CLK_50S	CLK	ISP1_CAM_FRONT_CLK 7 22
B9	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_F 22 60
D8	CLK_50S	CLK	ISP0_CAM_REAR_CLK_R 7
D10	CLK_50S	CLK	ISP0_CAM_REAR_CLK 7 23
D11	CLK_50S	CLK	ISP0_CAM_REAR_CLK_F 23 60

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
D10	UART_50S	UART	UART0_SOC_RXD 5 47 60
D9	UART_50S	UART	UART0_SOC_TXD 5 47 60
D14	UART_50S	UART	UART3_SOC2BB_RTS_L 5 25 29
D15	UART_50S	UART	UART3_BB2SOC_RTS_L 5 25 29
D13	UART_50S	UART	UART3_SOC2BB_TX 5 25 29 47
D12	UART_50S	UART	UART3_BB2SOC_TX 5 25 29 47
D16	UART_50S	UART	UART4_OSCAR2SOC_RXD 5 19
D17	UART_50S	UART	UART4_SOC2OSCAR_TXD 5 19
D18	UART_50S	UART	UART1_SOC2BT_RTS_L 5 46
D19	UART_50S	UART	UART1_BT2SOC_RTS_L 5 46
D20	UART_50S	UART	UART1_SOC2BT_TX 5 46
D21	UART_50S	UART	UART1_BT2SOC_TX 5 46
D22	UART_50S	UART	UART2_SOC2WLAN_TX 5 46
D23	UART_50S	UART	UART2_WLAN2SOC_TX 5 46
D24	UART_50S	UART	UART2_SOC2WLAN_TX_R 46 61
D25	UART_50S	UART	UART2_WLAN2SOC_TX_R 46 61
D26	UART_50S	UART	UART6_TS_ACC_RXD 5 47
D27	UART_50S	UART	UART6_TS_ACC_TXD 5 47
D28		UART	UART5_BATT_TRXD 5 54 57
D29		UART	BATT_SWI_CONN 54 60

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
A17	I2S_50S	CLK	I2S0_CODEC_ASP_MCK_R 5 15
A16	I2S_50S	CLK	I2S0_CODEC_ASP_MCK 5
A18	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 15
A14	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 15
A12	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 15
A11	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 15
A15	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 15
B11	I2S_50S	I2S	NC_I2S1_MCK 5
B15	I2S_50S	I2S	I2S1_CODEC_XSP_BCLK 5 15
B14	I2S_50S	I2S	I2S1_CODEC_XSP_LRCK 5 15
B13	I2S_50S	I2S	I2S1_CODEC_XSP_DIN 5 15
B12	I2S_50S	I2S	I2S1_CODEC_XSP_DOUT 5 15
B10	I2S_50S	I2S	I2S1_CODEC_XSP_SDOUT 15
C24	I2S_50S	CLK	NC_I2S2_MCK_R
C25	I2S_50S	CLK	NC_I2S2_MCK 5
C26	I2S_50S	I2S	NC_I2S2_BCLK 5
C27	I2S_50S	I2S	NC_I2S2_LRCK 5
C28	I2S_50S	I2S	NC_I2S2_DIN 5
C29	I2S_50S	I2S	NC_I2S2_DOUT 5
F20	I2S_50S	I2S	NC_I2S4_MCK 5
F21	I2S_50S	I2S	I2S4_SOC2BT_BCLK 5 46
F22	I2S_50S	I2S	I2S4_SOC2BT_LRCK 5 46
F23	I2S_50S	I2S	I2S4_SOC2BT_DATA 5 46
F24	I2S_50S	I2S	I2S4_BT2SOC_DATA 5 46

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
A32		DWI	DWI_AP_CLK 5 57
A34		DWI	NC_DWI_AP_DI 57
A35		DWI	DWI_AP_DO 5 57

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B1	I2C_50S	I2C	I2C0_SDA_1V8 5 57 60
B2	I2C_50S	I2C	I2C0_SCL_1V8 5 57 60
B3	I2C_50S	I2C	I2C3_CAM_ALS_SDA_1V8_F 22 60
B4	I2C_50S	I2C	I2C3_CAM_ALS_SCL_1V8_F 22 60
B5	I2C_50S	I2C	I2C0_HP_ALS_SDA_1V8_FILT 60
B6	I2C_50S	I2C	I2C0_HP_ALS_SCL_1V8_FILT 60
D31	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDCLK_1V8 5 19
D30	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDIO_1V8 5 19
D1	I2C_50S	I2C	I2C2_SDA_1V8 5 47
D2	I2C_50S	I2C	I2C2_SCL_1V8 5 47
D29	I2C_50S	I2C	I2C3_SDA_1V8 5 13 22 61
D28	I2C_50S	I2C	I2C3_SCL_1V8 5 13 22 61
D33	I2C_50S	I2C	DMIC1_FF_SD_FILT 16 60
D32	I2C_50S	I2C	DMIC1_FF_SCLK_FILT 16 60
D34	I2C_50S	I2C	DMIC1_FF_SD 15 16
D35	I2C_50S	I2C	DMIC1_FF_SCLK 15 16
D37	I2C_50S	I2C	SEP_I2C0_SCL 5
D36	I2C_50S	I2C	SEP_I2C0_SDA 5
B8	I2C_50S	I2C	ISP0_CAM_REAR_SCL 7 23
B9	I2C_50S	I2C	ISP0_CAM_REAR_SDA 7 23
B10	I2C_50S	I2C	ISP0_CAM_REAR_SCL_F 23 60
B11	I2C_50S	I2C	ISP0_CAM_REAR_SDA_F 23 60
D38	I2C_50S	I2C	ISP1_CAM_FRONT_SCL 7 22
D39	I2C_50S	I2C	ISP1_CAM_FRONT_SDA 7 22
D40	I2C_50S	I2C	ISP1_CAM_FRONT_SCL_F 22 60
D41	I2C_50S	I2C	ISP1_CAM_FRONT_SDA_F 22 60

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
D20	SPI_50S	SPI	SPI3_CODEC_MISO 5 15
D21	SPI_50S	SPI	SPI3_CODEC_MOSI 5 15
D19	SPI_50S	SPI	SPI3_CODEC_SCLK 5 15
D18	SPI_50S	SPI	SPI3_CODEC_CS_L 5 15
D24	SPI_50S	SPI	SPI2_GRAPE_MISO 5 52 60 61 64
D25	SPI_50S	SPI	SPI2_GRAPE_MOSI 5 52 60 61 64
D23	SPI_50S	SPI	SPI2_GRAPE_SCLK 5 52 60 61 64
D22	SPI_50S	SPI	SPI2_GRAPE_CS_L 5 52 60 61 64
B26	SPI_50S	SPI	SPI2_GRAPE_MISO 5 52 60 61 64
B27	SPI_50S	SPI	SPI2_GRAPE_MOSI 5 52 60 61 64
B28	SPI_50S	SPI	SPI2_GRAPE_SCLK 5 52 60 61 64
B29	SPI_50S	SPI	SPI2_GRAPE_CS_L 5 52 60 61 64
D17	SPI_50S	SPI	SPI_OSCAR_MISO 19 24
D16	SPI_50S	SPI	SPI_OSCAR_MOSI 19 24
D15	SPI_50S	SPI	SPI_OSCAR_SCLK 19 24
D14	SPI_50S	SPI	SPI_OSCAR_MISO_GYRO 19
D13	SPI_50S	SPI	SPI_OSCAR_MISO_ACCEL 19
D12	SPI_50S	SPI	SPI_OSCAR_MISO_COMP1 24
D27	SPI_50S	SPI	SPI_OSCAR_MOSI_R 19
D26	SPI_50S	SPI	SPI_OSCAR_SCLK_R 19
D28	SPI_50S	SPI	SPI_OSCAR2ACCEL_CS_L 19
D29	SPI_50S	SPI	SPI_OSCAR2GYRO_CS_L 19
D30	SPI_50S		SPI_OSCAR2COMPASS_CS_L 19 24

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B16		JTAG	JTAG_SOC_TCK 4 47 60
B17		JTAG	JTAG_SOC_TMS 4 47 60
B18		JTAG	JTAG_SOC_TDI 4 60
B19		JTAG	TP_JTAG_SOC_TDO 4 60
B20		RST	JTAG_SOC_TRST_L 4 13 60
B21		JTAG	NC_JTAG_SOC_TRTCK 4
D42		JTAG	BB_JTAG_TMS 5 25 28 61
D43		JTAG	BB_JTAG_TCK 5 25 28 61
D44		JTAG	BB_JTAG_TDO 5 25 28 61
D45		JTAG	BB_JTAG_TDI 5 25 28 61
D46		RST	BB_JTAG_TRST_L 5 25 28 61
B22		JTAG	JTAG_WLAN_TMS_TX_BLANK 46 61
B23		JTAG	TP_JTAG_WLAN_TCK 46 61
B24		JTAG	JTAG_WLAN_TDO_OSCAR_B 46 61
B25		JTAG	JTAG_WLAN_TDI_OSCAR_A 46 61
B30		RST	TP_JTAG_WLAN_TRST_L 46 61
B31		JTAG	TP_JTAG_CUMULUS_M_TCK 52 61
B32		JTAG	TP_JTAG_CUMULUS_M_TDI 52 61
B33		JTAG	JTAG_CUMULUS_M_TMS 52 61
B34		JTAG	TP_JTAG_CUMULUS_M_TDO 52 61

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B1	USB_90D	USB	USB_SOC_P 4 47 60
B2	USB_90D	USB	USB_SOC_N 4 47 60
D48	USB_90D	USB	USB_BB_P 25 47
D49	USB_90D	USB	USB_BB_N 25 47
D50	USB_90D	USB	USB_BB_DEBUG_P 25 28 61
D51	USB_90D	USB	USB_BB_DEBUG_N 25 28 61
D52	USB_90D	USB	E75_DPAIR1_CONN_P 47 49 60
D53	USB_90D	USB	E75_DPAIR1_CONN_N 47 49 60
D54	USB_90D	USB	E75_DPAIR2_CONN_P 47 49 60
D55	USB_90D	USB	E75_DPAIR2_CONN_N 47 49 60
D56	USB_90D	USB	E75_DPAIR1_P 47
D57	USB_90D	USB	E75_DPAIR1_N 47
D58	USB_90D	USB	E75_DPAIR2_P 47
D59	USB_90D	USB	E75_DPAIR2_N 47

HSIC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC	GND	*	1.5:1_SPACING
HSIC_RDY	*	*	2:1_SPACING
HSIC_RDY	GND	*	1.5:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
D31	HSIC	HSIC	HSIC1_WLAN_DATA 4 46 61
D34	HSIC	HSIC	HSIC1_WLAN_STB 4 46 61
D33	HSIC	HSIC	HSIC2_BB_DATA 4 25 28 61
D32	HSIC	HSIC	HSIC2_BB_STB 4 25 28 61
D27	HSIC	HSIC	NC_HSIC0_DATA 4
D26	HSIC	HSIC	NC_HSIC0_STB 4
D35	HSIC	HSIC_RDY	HSIC1_WLAN2SOC_REMOTE_WAKE 5 46 61
D36	HSIC	HSIC_RDY	HSIC1_WLAN2SOC_DEVICE_RDY 5 46 61
D37	HSIC	HSIC_RDY	HSIC1_SOC2WLAN_HOST_RDY 5 46
D29	HSIC	HSIC_RDY	HSIC1_SOC2WLAN_HOST_RDY_R 46 61
D30	HSIC	HSIC_RDY	HSIC2_BB2SOC_REMOTE_WAKE 5 29
D39	HSIC	HSIC_RDY	HSIC2_BB2SOC_DEVICE_RDY 5 25 29
D40	HSIC	HSIC_RDY	HSIC2_SOC2BB_HOST_RDY 5 25 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_P	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_N	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_P<0>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_N<0>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_P<1>	7 23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_N<1>	7 23 61
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_P<2>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_N<2>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_P<3>	7
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_N<3>	7
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_FILT_P	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_CLK_FILT_N	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_P<0>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_N<0>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_P<1>	23 61
	MIPI_90D	MIPI0C	MIPI0C_CAM_REAR_DATA_FILT_N<1>	23 61
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<2>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<2>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<3>	
	MIPI_90D	MIPI0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<3>	
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_P	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_N	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_P<0>	7 22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_N<0>	7 22 61
	MIPI_90D	MIPI1C	NC_MIPI1C_CAM_FRONT_DATA_P<1>	7
	MIPI_90D	MIPI1C	NC_MIPI1C_CAM_FRONT_DATA_N<1>	7
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_FILT_P	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_CLK_FILT_N	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_FILT_P<0>	22 61
	MIPI_90D	MIPI1C	MIPI1C_CAM_FRONT_DATA_FILT_N<0>	22 61
	MIPI_90D	MIPI1C	NC_MIPI0D_DPCLK	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNCLK	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA0	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA0	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA1	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA1	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA2	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA2	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DPDATA3	7
	MIPI_90D	MIPI1C	NC_MIPI0D_DNDATA3	7
	MIPI_90D	MIPI0C	MIPI_CAM0_CLKCON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_CLKCON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D0CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D0CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D1CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D1CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D2CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D2CON_N	
	MIPI_90D	MIPI0C	MIPI_CAM0_D3CON_P	
	MIPI_90D	MIPI0C	MIPI_CAM0_D3CON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_CLKCON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_CLKCON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_D0CON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_D0CON_N	
	MIPI_90D	MIPI1C	MIPI_CAM1_D1CON_P	
	MIPI_90D	MIPI1C	MIPI_CAM1_D1CON_N	

DEV

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	2.4:1_SPACING
LEDB	*	*	2.4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LED	LEDA	LED_IO1_A_R	56
	LED	LEDB	LED_IO1_B_R	56
	LED	LEDA	LED_IO2_A_R	56
	LED	LEDB	LED_IO2_B_R	56
	LED	LEDA	LED_IO3_A_R	56
	LED	LEDB	LED_IO3_B_R	56
	LED	LEDA	LED_IO4_A_R	56
	LED	LEDB	LED_IO4_B_R	56
	LED	LEDA	LED_IO5_A_R	56
	LED	LEDB	LED_IO5_B_R	56
	LED	LEDA	LED_IO6_A_R	56
	LED	LEDB	LED_IO6_B_R	56
	LED	LEDA	LED_IO_1_A	53 56 60
	LED	LEDB	LED_IO_1_B	53 56 60
	LED	LEDA	LED_IO_2_A	53 56 60
	LED	LEDB	LED_IO_2_B	53 56 60
	LED	LEDA	LED_IO_3_A	53 56 60
	LED	LEDB	LED_IO_3_B	53 56 60
	LED	LEDA	LED_IO_4_A	53 56 60
	LED	LEDB	LED_IO_4_B	53 56 60
	LED	LEDA	LED_IO_5_A	53 56 60
	LED	LEDB	LED_IO_5_B	53 56 60
	LED	LEDA	LED_IO_6_A	53 56 60
	LED	LEDB	LED_IO_6_B	53 56 60

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING
AUDIO	AUDIO	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L1_OUT_P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L1_OUT_N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L2_OUT_P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_L2_OUT_N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R1_OUT_P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R1_OUT_N	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R2_OUT_P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP_R2_OUT_N	17 49 60
	USB_90D	USB	MIKEY_TS_P	15 47
	USB_90D	USB	MIKEY_TS_N	15 47
MAXIMUM_NECK_LENGTH=0.5 MM MIN_NECK_WIDTH=0.06 MM	USB_90D	USB	L81_MBUS_P	15
	USB_90D	USB	L81_MBUS_N	15
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT_CH_OUT_P	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT_CH_OUT_N	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT_CH_OUT_P	15 17 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT_CH_OUT_N	15 17 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L1_IN_P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L1_IN_N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R1_IN_P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R1_IN_N	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L2_IN_P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_L2_IN_N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R2_IN_P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304_R2_IN_N	17 61
	AUDIO_DIFF	AUDIO	SPKR_L1_VSNS_P	
	AUDIO_DIFF	AUDIO	SPKR_L1_VSNS_N	
	AUDIO_DIFF	AUDIO	SPKR_R1_VSNS_P	
	AUDIO_DIFF	AUDIO	SPKR_R1_VSNS_N	
MAXIMUM_NECK_LENGTH=15 MM	PWR_0P5MM	AUDIO	CODEC_HP_HS3	15
	PWR_0P5MM	AUDIO	CODEC_HP_HS4	15
	PWR_0P5MM	AUDIO	CONN_HP_HS3_FILT	15 16 60
	PWR_0P5MM	AUDIO	CONN_HP_HS4_FILT	15 16 60
	PWR_0P2MM	AUDIO	CODEC_HP_LEFT	15
	PWR_0P2MM	AUDIO	CODEC_HP_RIGHT	15
	PWR_0P2MM	AUDIO	CONN_HP_LEFT_FILT	15 16 60
	PWR_0P2MM	AUDIO	CONN_HP_RIGHT_FILT	15 16 60
	PP_PWR	PWR	L81_NVCP	15 61
	PP_PWR	PWR	L81_PVCP	15 61
	PP_PWR	PWR	L81_FLYP	15 61
	PP_PWR	PWR	L81_FLYN	15 61
	PP_PWR	PWR	L81_FLYC	15 61
	PP_PWR	PWR	SPEAKER_VQ	
	PP_PWR	PWR	L81_FILT	15
	PWR_0P1MM	AUDIO	HP_MIC_POS	15
	PWR_0P1MM	AUDIO	HP_MIC_NEG	15
	PWR_0P1MM	AUDIO	L81_AIN2_POS	15
	PWR_0P1MM	AUDIO	L81_AIN2_NEG	15
	PWR_0P1MM	AUDIO	CODEC_HP_HS3_REF	15
	PWR_0P1MM	AUDIO	CODEC_HP_HS4_REF	15
	PWR_0P1MM	AUDIO	CONN_HP_HS3_REF_FILT	15 16 60
	PWR_0P1MM	AUDIO	CONN_HP_HS4_REF_FILT	15 16 60

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		CRYSTAL	XTAL_SOC_24M_I	4
		CRYSTAL	XTAL_SOC_24M_O	4
		CRYSTAL	SOC_24M_O	4
		CRYSTAL	PMU_XTAL	56
		CRYSTAL	PMU_EXTAL	56

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	EDP_90D	EDP	EDP_AUX_P	7 53
	EDP_90D	EDP	EDP_AUX_N	7 53
	EDP_50S	EDP	EDP_HPD	7 53
EDP	EDP_90D	EDP	EDP_DATA_P<0>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<0>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<1>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<1>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<2>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<2>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_P<3>	7 53 61
EDP	EDP_90D	EDP	EDP_DATA_N<3>	7 53 61
	EDP_90D	EDP	EDP_AUX_EMI_P	53
	EDP_90D	EDP	EDP_AUX_EMI_N	53
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_P<3>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_N<3>	53 61
	EDP_90D	EDP	EDP_AUX_EMI_CONN_P	53
	EDP_90D	EDP	EDP_AUX_EMI_CONN_N	53
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<0>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<1>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<2>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_P<3>	53 61
EDP	EDP_90D	EDP	EDP_DATA_EMI_CONN_N<3>	53 61

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	BOARD_TEMP	BOARD_TEMP	PA_NTC_P	57 60
MIN_NECK_WIDTH=0.053 MM	BOARD_TEMP	BOARD_TEMP	PA_NTC_N	57
MIN_NECK_WIDTH=0.053 MM	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP2_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP2_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	57
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	57 60
	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	57

GRAPE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GRAPE	*	GRAPE_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GRAPE	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	GRAPE	GRAPE	MT_PANEL_IN<0..29>	52 61
	GRAPE	GRAPE	MT_PANEL_OUT<0..39>	52 61

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DRAM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DRAM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1233	DDR_50S	DDR	DDR0_CA<0>	8 12 61
1221	DDR_50S	DDR	DDR0_CA<9..1>	8 12 61
1222	DDR_50S	DDR	DDR0_DM<3..0>	8 12 61
1223	DDR_90D	DDR	DDR0_CK_P	8 12 61
1225	DDR_90D	DDR	DDR0_CK_N	8 12 61
1226	DDR_50S	DDR	DDR0_CKE<1..0>	8 12 61
1224	DDR_50S	DDR	DDR0_CSN<1..0>	8 12 61
1229		DDR	DDR0_CA_ZQ_SOC	8
1227		DDR	DDR0_DQ_ZQ_SOC	8
1204		DDR	DDR0_ZQ_DRAM	12
1230	DDR_50S	DDR	DDR0_DQ<1..0>	8 12 61
1232	DDR_50S	DDR	DDR0_DQ<2>	8 12 61
1235	DDR_50S	DDR	DDR0_DQ<7..3>	8 12 61
1228	DDR_90D	DDR	DDR0_DQS_P<0>	8 12 61
1231	DDR_90D	DDR	DDR0_DQS_N<0>	8 12 61
1234	DDR_50S	DDR	DDR0_DQ<15..8>	8 12 61
1233	DDR_90D	DDR	DDR0_DQS_P<1>	8 12 61
1235	DDR_90D	DDR	DDR0_DQS_N<1>	8 12 61
1234	DDR_50S	DDR	DDR0_DQ<23..16>	8 12 61
1236	DDR_90D	DDR	DDR0_DQS_P<2>	8 12 61
1237	DDR_90D	DDR	DDR0_DQS_N<2>	8 12 61
1238	DDR_50S	DDR	DDR0_DQ<27..25>	8 12 61
1238	DDR_50S	DDR	DDR0_DQ<28>	8 12 61
1239	DDR_50S	DDR	DDR0_DQ<31..29>	8 12 61
1239	DDR_90D	DDR	DDR0_DQS_P<3>	8 12 61
1240	DDR_90D	DDR	DDR0_DQS_N<3>	8 12 61
1238	DDR_50S	DDR	DDR1_CA<3..0>	8 12 61
1201	DDR_50S	DDR	DDR1_CA<9..4>	8 12 61
1202	DDR_50S	DDR	DDR1_DM<3..0>	8 12 61
1203	DDR_90D	DDR	DDR1_CK_P	8 12 61
1205	DDR_90D	DDR	DDR1_CK_N	8 12 61
1206	DDR_50S	DDR	DDR1_CKE<1..0>	8 12 61
1204	DDR_50S	DDR	DDR1_CSN<0>	8 12 61
1239	DDR_50S	DDR	DDR1_CSN<1>	8 12 61
1238		DDR	DDR1_CA_ZQ_SOC	8
1201		DDR	DDR1_DQ_ZQ_SOC	8
1207		DDR	DDR1_ZQ_DRAM	12
1210	DDR_50S	DDR	DDR1_DQ<7..0>	8 12 61
1209	DDR_90D	DDR	DDR1_DQS_P<0>	8 12 61
1211	DDR_90D	DDR	DDR1_DQS_N<0>	8 12 61
1212	DDR_50S	DDR	DDR1_DQ<15..8>	8 12 61
1213	DDR_90D	DDR	DDR1_DQS_P<1>	8 12 61
1215	DDR_90D	DDR	DDR1_DQS_N<1>	8 12 61
1214	DDR_50S	DDR	DDR1_DQ<23..16>	8 12 61
1216	DDR_90D	DDR	DDR1_DQS_P<2>	8 12 61
1217	DDR_90D	DDR	DDR1_DQS_N<2>	8 12 61
1218	DDR_50S	DDR	DDR1_DQ<31..24>	8 12 61
1219	DDR_90D	DDR	DDR1_DQS_P<3>	8 12 61
1220	DDR_90D	DDR	DDR1_DQS_N<3>	8 12 61

VREF (DDR/FMI)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MIN_NECK_WIDTH=0.15 MM			
0.6V	PP_PWR	PWR	PPVREF_DDR0_CA_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR0_CA_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_DRAM	12
0.9V	PP_PWR	VREF	PPVREF_FMI_SOC	6 61
0.9V	PP_PWR	VREF	PPVREF_FMI_NAND	14 61

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
568	FMI0_AD_CTRL_PP	NAND_50S	NAND	FMI0_AD<0>	6 14 61
569	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<1>	6 14 61
570	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<2>	6 14 61
571	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<3>	6 14 61
572	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<4>	6 14 61
573	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<5>	6 14 61
574	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<6>	6 14 61
575	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<7>	6 14 61
576	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_ALE	6 14 61
577	FMI0_CE	NAND_50S	NAND	FMI0_CE0_L	6 14 60 61
578	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_CLE	6 14 61
1328		NAND_50S	NAND	FMI0_DQS	6 14 61
1331	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_RE_L	6 14 61
1333	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_WE_L	6 14 61
1135	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<0>	6 14 61
1136	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<1>	6 14
1137	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<2>	6 14
1138	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<3>	6 14
1139	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<4>	6 14
1140	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<5>	6 14
1141	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<6>	6 14
1142	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<7>	6 14
1143	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_ALE	6 14 61
1144	FMI1_CE	NAND_50S	NAND	FMI1_CE0_L	6 14 61
1152	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_CLE	6 14 61
1154	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_DQS	6 14 61
1156	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_RE_L	6 14 61
1160	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_WE_L	6 14 61

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
1305	NAND_50S	NAND	FMI0_AD_BUF<0>
1307	NAND_50S	NAND	FMI0_AD_BUF<1>
1306	NAND_50S	NAND	FMI0_AD_BUF<2>
1308	NAND_50S	NAND	FMI0_AD_BUF<3>
1309	NAND_50S	NAND	FMI0_AD_BUF<4>
1300	NAND_50S	NAND	FMI0_AD_BUF<5>
1302	NAND_50S	NAND	FMI0_AD_BUF<6>
1304	NAND_50S	NAND	FMI0_AD_BUF<7>
1303	NAND_50S	NAND	FMI0_ALE_BUF
1301	NAND_50S	NAND	FMI0_CE0_BUF_L
1324	NAND_50S	NAND	FMI0_CLE_BUF
1326	NAND_50S	NAND	FMI0_DQS_BUF
1327	NAND_50S	NAND	FMI0_DQSN_BUF
1328	NAND_50S	NAND	FMI0_REP_BUF
1329	NAND_50S	NAND	FMI0_RE_BUF_L
1330	NAND_50S	NAND	FMI0_WE_BUF_L
1311	NAND_50S	NAND	FMI1_AD_BUF<0>
1312	NAND_50S	NAND	FMI1_AD_BUF<1>
1314	NAND_50S	NAND	FMI1_AD_BUF<2>
1313	NAND_50S	NAND	FMI1_AD_BUF<3>
1315	NAND_50S	NAND	FMI1_AD_BUF<4>
1316	NAND_50S	NAND	FMI1_AD_BUF<5>
1317	NAND_50S	NAND	FMI1_AD_BUF<6>
1318	NAND_50S	NAND	FMI1_AD_BUF<7>
1319	NAND_50S	NAND	FMI1_ALE_BUF
1320	NAND_50S	NAND	FMI1_CE0_BUF_L
1322	NAND_50S	NAND	FMI1_CLE_BUF
1323	NAND_50S	NAND	FMI1_DQS_BUF
1321	NAND_50S	NAND	FMI1_DQSN_BUF
1324	NAND_50S	NAND	FMI1_REP_BUF
1325	NAND_50S	NAND	FMI1_RE_BUF_L
1326	NAND_50S	NAND	FMI1_WE_BUF_L

PWR

	VOLTAGE	PHYSICAL	SPACING	
				BUCKS
J223	4.7V	PP_PWR	PWR	BUCK0_LX0 55
J1	4.7V	PP_PWR	PWR	BUCK0_LX1 55
J2	4.7V	PP_PWR	PWR	BUCK0_LX2 55
J3	4.7V	PP_PWR	PWR	BUCK0_LX3 55
J4	1.1V	PP_PWR	PWR	BUCK0_FB 55
J5	4.7V	PP_PWR	PWR	BUCK1_LX0 55
J6	4.7V	PP_PWR	PWR	BUCK1_LX1 55
J7	4.7V	PP_PWR	PWR	BUCK1_LX2 55
J8	1.1V	PP_PWR	PWR	BUCK1_FB 55
J9	4.7V	PP_PWR	PWR	BUCK2_LX0 55
J12	1.0V	PP_PWR	PWR	BUCK2_FB 55
J13	4.7V	PP_PWR	PWR	BUCK3_LX0 55
J10	1.8V	PP_PWR	PWR	BUCK3_FB 55
J11	4.7V	PP_PWR	PWR	BUCK4_LX0 55
J15	1.2V	PP_PWR	PWR	BUCK4_FB 55
J14	4.7V	PP_PWR	PWR	BUCK5_LX0 55
J16	1.0V	PP_PWR	PWR	BUCK5_FB 55
J17	4.7V	PP_PWR	PWR	BUCK6_LX0 55
J19	3.3V	PP_PWR	PWR	BUCK6_FB 55
				RAILS
J368	1.1V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVDD_CPU 55 60 62
J19	1.1V	MIN_NECK_WIDTH=0.15 MM PWR_10MM	PWR	PPVDD_GPU 55 60 62
J20	1.0V	MIN_NECK_WIDTH=0.15 MM PWR_2MM	PWR	PPVDD_SOC 55 60 62
J21	1.8V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V8_S2R 55 56 60 62
J25	1.8V	MAX_LINE_WIDTH=0.6 MM PWR_0P3MM	PWR	PP1V8_SW1 55 57 59 60 62
J364	1.8V	MAXIMUM_NECK_LENGTH=10 MM PWR_0P5MM	PWR	PP1V8_SW1_FOREHEAD 60 62
J30	1.8V	MIN_NECK_WIDTH=0.15 MM PP_PWR	PWR	PP1V8_EXT_SW 57 60 62
J34	1.8V	PWR_0P1MM	PWR	PP1V8_SW2 55 60 62
J28	1.8V	PP_PWR	PWR	PP1V8_S2R_SW3 55 60 62
J365	1.8V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP1V8_S2R_SW3_COMP 60 62
J23	1.2V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP1V2_S2R 55 56 60 62
J29	1.2V	PWR_1MM	PWR	PP1V2_SW1 55 60 62
J367	1.2V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V2_S2R_SW2 55 60 62
J22	3.3V	MIN_NECK_WIDTH=0.1 MM PWR_1MM	PWR	PPVDD_SRAM 55 60 62
J24	3.3V	PWR_1P2MM	PWR	PP3V3_S2R 55 60 62
J25	3.3V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP3V3_SW 57 60 62
				LDOS
J288	3.0V	MAXIMUM_NECK_LENGTH=20 MM PP_PWR	PWR	PP3V0_SPARE1 56 60 62
J31	1.7V	PP_PWR	PWR	PP1V7_VA_VCP 56 60 62
J36	3.0V	MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP3V0_S2R_SENSOR 56 60 62
J273	3.0V	MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM	PWR	PP3V0_ALS 56 60 62
J35	3.0V	PWR_0P4MM	PWR	PP3V0_UVLO 56 60 62
J222	3.3V	PP_PWR	PWR	PP3V3_ACC 56 60 62
J33	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_TRISTAR 56 60 62
J32	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_HALL 56 60 62
J37	1.3V	MAXIMUM_NECK_LENGTH=7 MM PP_PWR	PWR	PP1V3_CAM 56 60 62
J38	1.0V	MAXIMUM_NECK_LENGTH=15 MM PP_PWR	PWR	PP1V0_SOC 56 60 62
J39	2.6V	MAXIMUM_NECK_LENGTH=45 MM PP_PWR	PWR	PP2V6_CAM_AF 56 60 62
J40	2.9V	MAXIMUM_NECK_LENGTH=40 MM PP_PWR	PWR	PP2V9_CAM 56 60 62
J374	5.25V	MAXIMUM_NECK_LENGTH=5 MM PP_PWR	PWR	PP5V25_GRAPE 56 60 62
				INPUT/MAIN/ALWAYS
J43	4.7V	MIN_NECK_WIDTH=0.15 MM PWR_15MM	PWR	PPVCC_MAIN 47 55 56 57 58 60 62
J45	4.7V	MAXIMUM_NECK_LENGTH=15 MM PWR_10MM	PWR	PPBATT_VCC 55 60 62
J58	6.0V	PWR_2MM	PWR	PPVBUS_USB_DCIN 55 60 62
J41	1.8V	MAX_LINE_WIDTH=0.6 MM PWR_0P2MM	PWR	PP1V8_ALWAYS 56 60 62
J300	4.7V	PWR_10MM	PWR	PPBATT_AUDIO_AMP
				PMU
J51	20.4V	PP_PWR	PWR	WLED_LX_B 56 61
J47	20.4V	PP_PWR	PWR	WLED_LX_A 56 61
J49	20.4V	MAX_LINE_WIDTH=0.6 MM PWR_0P5MM	PWR	PPLED_OUT_A 56 60 62
J50	20.4V	MAX_LINE_WIDTH=0.6 MM PWR_0P5MM	PWR	PPLED_OUT_B 56 60 62
J229	20.4V	PWR_PMU	PWR	PPLED_BACK_REG_A 53 60
J230	20.4V	PWR_PMU	PWR	PPLED_BACK_REG_B 53 60
J54	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 56 60
J55	6.0V	PWR_0P2MM	PWR	PPVBUS_PROT 47 55 60
J57	6.0V	PP_PWR	PWR	PMU_VCENTER 55 60
J53	6.0V	PP_PWR	PWR	PP6V0_LCM_HI 56 61
J52	20.4V	PP_PWR	PWR	LCM_LX 56
J60	4.7V	PP_PWR	PWR	SW_CHGA 55 61
J56	6.0V	PWR_0P2MM	PWR	USB_VBUS_DETECT 4 55
J289	6.0V	PWR_0P2MM	PWR	USB_VBUS_DETECT_R 4
J266	6.0V		PWR	PMU_GPIO_BB_VBUS_DET 25 28 57 61

	VOLTAGE	PHYSICAL	SPACING	
J61	1.8V	PP_PWR	PWR	PP1V8_PLL_SOC_F 4
J62	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
J206	0.4V	PP_PWR	PWR	TP_PP0V4_MIPI0D 7
J205	0.4V	PP_PWR	PWR	TP_PP0V4_MIPI1D 7
J200	1.8V	PWR_0P2MM	PWR	PP1V8_XTAL 9
J201	1.8V	PP_PWR	PWR	PP1V8_VDD_ANA_TMPSADC 10
J240	1.2V	PP_PWR	PWR	PPVDDI_NAND 14
J63	1.8V	PP_PWR	PWR	PP1V8_DMIC_FILT 16 60
J64	3.0V	PP_PWR	PWR	PP3V0_HP_ALS_FILT 60
J214	8.75V	PP_PWR	PWR	SPKR_L1_SWITCH
J213	8.75V	PP_PWR	PWR	SPKR_R1_SWITCH
J177	1.8V	PP_PWR	PWR	PPDVDD_SPKRAMP
J65	1.7V	PP_PWR	PWR	PP1V7_VCP 15 60
J66	4.2V	PP_PWR	PWR	PPVCC_VPROG_CP 15
J209	4.2V	PP_PWR	PWR	PPVCC_VPROG_MB
J208	4.2V	PP_PWR	PWR	PPVCC_VPROG_MB_F 15
J67	4.7V	PWR_1MM	PWR	PPVCC_MAIN_LCD_SW 53 60
J68	4.7V	PWR_1MM	PWR	PPVCC_MAIN_LCD_SW_CONN 53 60
J69	4.7V	PWR_1MM	PWR	PPVCC_MAIN_GRAPE_FILT
J373	5.25V	PP_PWR	PWR	PP5V25_GRAPE_FILT
J70	1.8V	PP_PWR	PWR	PP1V8_GRAPE_SW 51 52 60 61
J71	1.8V	PP_PWR	PWR	PP1V8_GRAPE_FILT
J72	3.0V	PP_PWR	PWR	PP3V0_GYRO 19 60
J73	3.0V	PP_PWR	PWR	PP3V0_ACCEL 19 60
J202	3.0V	PWR_0P3MM	PWR	PP3V0_S2R_HALL_FILT 20 50 60
J203	1.2V	PWR_0P3MM	PWR	PP1V2_CAM_FRONT_FILT 60
J204	1.8V	PP_PWR	PWR	PP1V8_CAM_FRONT_FILT 22 60
J74	2.9V	PP_PWR	PWR	PP2V9_AVDD_CAM_FRONT_FILT 22 60
J75	3.0V	PWR_0P3MM	PWR	PP3V0_ALS_FILT 22 60
J227	2.6V	PP_PWR	PWR	PP2V6_CAM_REAR_AF_FILT 23 60
J207	1.28V	PP_PWR	PWR	PP1V3_CAM_REAR_FILT 23 60
J210	1.8V	PP_PWR	PWR	PP1V8_CAM_REAR_FILT 23 60
J228	1.28V	PP_PWR	PWR	PP1V3_CAM_REAR
J226	2.8V	PP_PWR	PWR	PP2V9_AVDD_CAM_REAR_FILT 23 60
J76	3.0V	PP_PWR	PWR	PP3V0_COMP 24 60
J77	1.8V	PP_PWR	PWR	PP1V8_COMP 24 60
J78	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_FILT 60
J79	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_ADUX1049_FILT 60
J80	3.0V	PP_PWR	PWR	PPAVDD_SENSOR_PROX_ADUX1049
J81	3.0V	PP_PWR	PWR	PP3V0_SENSOR_PROX_AD7149_FILT 45 60
J82	6.0V	PWR_2MM	PWR	PPVBUS_E75_USB_CONN 48 49 60
J83	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID1_CONN 48 49 60
J84	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID2_CONN 48 49 60
J85	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID1 47 48
J86	3.3V	PP_PWR	PWR	PPOUT_E75_ACC_ID2 47 48
J87	3.0V	PP_PWR	PWR	PP3V0_IO_ALS_FILT 60
J88			ANLG	BATT_NTC 54 57 60
J89		MAXIMUM_NECK_LENGTH=20 MM PP_PWR	ANLG	BATT_SNS 54 55
J90		MAXIMUM_NECK_LENGTH=5 MM PP_PWR	ANLG	BATT_SNS_R 55

GND

VOLTAGE	PHYSICAL	SPACING	
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AUDIO_CODEC 15 60
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_AVDD_CAM_FRONT 22
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP1V8_CAM_FRONT 22
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_PP2V9_CAM_FRONT 22
0V	MAX_LINE_WIDTH=0.6 MM GND	GND	GND_COMP 24
0V	GND	GND	GND_PMU
0V	GND	GND	GND_SPKR_AMP_L1
0V	GND	GND	GND_SPKR_AMP_L2
0V	GND	GND	GND_SPKR_AMP_R1
0V	GND	GND	GND_SPKR_AMP_R2

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		RST	BB_TRST_L
		RST	DBG_RST DEV
		RST	DEBUG_RST_L 25 28 61
		RST	GSM_TXBURST_IND
		RST	RST_AP_1V8_L
		RST	RESET_SOC_L 4 13 25 47 57 60 61
		RST	GPIO_SOC2BB_RST_L 5 25 27 60
		RST	RST_BB_PMU_L
		RST	RST_BT_L
		RST	RST_DET_L
		RST	GPIO_SOC2GRAPE_RESET_L 5 52 60 61
		RST	PMU_GPIO_CODEC_RST_L 15 57
		RST	TS2PMU_RESET_IN 47 57
		RST	GPIO_BB2SOC_RESET_DET_L 5 25 29
		RST	SIMCRD_RST
		RST	WDOG_SOC 4 13
		RST	WDOG_SOC2PMU_RESET_IN 13 57
		RST	GPIO_OSCAR_RESET_L 5 19 60
		RST	ISP1_CAM_FRONT_SHUTDOWN_L 7 22
		RST	ISP0_CAM_REAR_SHUTDOWN_L 7 23
		RST	ISP1_CAM_FRONT_SHUTDOWN_L_F 22 60
		RST	ISP0_CAM_REAR_SHUTDOWN_L_F 23 60
		RST	PMU_GPIO_PMU2BBPMU_RST_L 25 27 57 60
		RST	PMU_GPIO_PMU2BBPMU_RST_R_L 57
		RST	JTAG_AP_TRST_L
		RST	GPIO_BB_RST_L
		RST	RST_PMU_IN
		RST	UD881_RST DEV
		RST	UD882_RST DEV

PMU SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PMU_SENSE	*	*	3:1_SPACING
PMU_SENSE	GND	*	1.5:1_SPACING

VOLTAGE	PHYSICAL	SPACING	
1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_SOC_SENSE 11 57 61
1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_SOC_SENSE 11 57 61
1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_SOC_SENSE 10 57 61
1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_RAIL_SENSE 11 57
1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_RAIL_SENSE 11 57
1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_RAIL_SENSE 10 57
1.05V	MIN_NECK_WIDTH=0.053 MM PWR_SENSE	PMU_SENSE	ADC_SMPS1_MSMC_1V05
1.8V	MIN_NECK_WIDTH=0.053 MM PWR_SENSE	PMU_SENSE	ADC_SMPS3_MSME_1V8

RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
RF_50S	*	50_OHM_RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
RF_100D	*	100_OHM_RF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
100_RF	*	*	100_RF_CLEAR_SPACING
50_RF	*	*	50_RF_SPACING
50_RF_CLEAR	*	*	50_RF_CLEAR_SPACING
RF_60	*	*	1.2:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	SPACING		
3	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_2G_FEM	40
4	3.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_PA	34 35 36 37 38 39 40
37	1.8V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LVS1	26 28
5	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF1_1V3_DRX_FE	31
6	4.7V UNDEFINED	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VREG	26
8	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF2_2V05_DRX_BB	31
9	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_PA_DCDC	
538	1.8V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO1	26 60
611	1.8V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO2_XO_HS_1V8	26 28
612	1.8V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO3_AMUX_1V8	26 27 28
613	3.3V	MAX_LINE_WIDTH=1 MM PWR_0P25MM	PWR_RF	PP_LDO4_VDDA_3V3	26 28
614	2.5V	MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO5_GPS_LNA_2V5	26 42
615	1.8V	MAXIMUM_NECK_LENGTH=5 MM MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM	PWR_RF	PP_LDO6_RUIM_1V8	26 28 44 60
2309	1.8V	MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM	PWR_RF	PP_LDO6_RUIM_1V8_FILT	44
617	1.8V	MAX_LINE_WIDTH=1 MM PWR_0P25MM	PWR_RF	PP_LDO7_DAC_1V8	26 28
618	1.2V	MAXIMUM_NECK_LENGTH=9 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM	PWR_RF	PP_LDO8_VDDPX_1V2	26 28
619	1.05V	MAX_LINE_WIDTH=1 MM PWR_0P75MM	PWR_RF	PP_LDO9_PLL_1V05	26 28
620	1.05V	MAX_LINE_WIDTH=1 MM PWR_0P75MM	PWR_RF	PP_LDO10_ADSP_1V05	26 28
621	1.05V	MAX_LINE_WIDTH=1 MM PWR_0P75MM	PWR_RF	PP_LDO11_MDSP_FW_1V05	26 28
624	1.05V	MAX_LINE_WIDTH=1 MM PWR_0P75MM	PWR_RF	PP_LDO12_MDSP_SW_1V05	26 28
623	2.95V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO13_VDDPX_2V95	26 28
622	2.65V	MAXIMUM_NECK_LENGTH=4 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RF	PP_LDO14_2V65	26 33 40 41
626	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S1	26
627	1.05V	MAX_LINE_WIDTH=1 MM PWR_0P75MM	PWR_RF	PP_SMPS1_MSMC_1V05	26 28 60
625	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S2	26
629	1.3V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS2_RF1_1V3	26 28 31 60
628	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S3	26
630	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_RF1_1V8_DIG	31
2718	1.8V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS3_MSME_1V8_FILT	29
632	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S4	26
631	2.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS4_RF2_2V05	26 31 60
633	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_VSW_S5	26
634	1.05V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_SMPS5_DSP_1V05	26 60
2234	4.7V	MAX_LINE_WIDTH=1 MM PWR_RF	PWR_RF	PP_BATT_VCC_PA_DCDC_IN2	

	NET_TYPE PHYSICAL	SPACING		
2001	45_OHM_SE	RF_60	50_HSIC_CAL	28
635	RF_50S	50_RF_CLEAR	50_XCVR_B13_B17_B20_TX	30 33
636	RF_50S	50_RF	50_XCVR_2G_LB_TX	30 40
637	RF_50S	50_RF_CLEAR	50_XCVR_B8_TX	30 33
638	RF_50S	50_RF_CLEAR	50_XCVR_B5_B18_TX	30 33
639	RF_50S	50_RF_CLEAR	50_XCVR_B2_B25_TX	30 32
640	RF_50S	50_RF	50_XCVR_2G_HB_TX	30 40
641	RF_50S	50_RF_CLEAR	50_XCVR_B3_B4_TX	30 32
642	RF_50S	50_RF_CLEAR	50_XCVR_B1_TX	30 32
643	RF_50S	50_RF	50_PDET_IN	30
644	RF_50S	50_RF_CLEAR	50_PDET_PAD_OUT	30
645	RF_50S	50_RF_CLEAR	50_PDET_PAD_IN	30 40
646	RF_50S	50_RF_CLEAR	50_B1_TX_SAW_IN	32 33
647	RF_50S	50_RF_CLEAR	50_B3_B4_TX_SAW_IN	32 33
648	RF_50S	50_RF_CLEAR	50_B2_B25_TX_SAW_IN	32 33
727	RF_50S	50_RF_CLEAR	50_B1_TX_SAW_OUT	33 34
728	RF_50S	50_RF_CLEAR	50_B2_TX_SAW_OUT	33 35
729	RF_50S	50_RF_CLEAR	50_B3_TX_SAW_OUT	33 35
730	RF_50S	50_RF_CLEAR	50_B4_TX_SAW_OUT	33 34
731	RF_50S	50_RF_CLEAR	50_B5_TX_SAW_OUT	33 37
732	RF_50S	50_RF_CLEAR	50_B8_TX_SAW_OUT	33 37
733	RF_50S	50_RF_CLEAR	50_B13_TX_SAW_OUT	33 38
734	RF_50S	50_RF_CLEAR	50_B17_TX_SAW_OUT	33 38
735	RF_50S	50_RF_CLEAR	50_B20_TX_SAW_OUT	33 36
651	RF_50S	50_RF_CLEAR	50_PCS_RX	
650	RF_50S	50_RF	50_PCS_RX_MATCH	
652	RF_50S	50_RF_CLEAR	50_DCS_RX	
653	RF_50S	50_RF_CLEAR	50_DCS_RX_MATCH	

	NET_TYPE PHYSICAL	SPACING		
588	RF_50S	50_RF_CLEAR	50_B1_TX_PAD_IN	34
587	RF_50S	50_RF_CLEAR	50_B4_TX_PAD_IN	34
589	RF_50S	50_RF_CLEAR	50_B1_B4_DPLX_ANT	34
590	RF_50S	50_RF_CLEAR	50_B1_B4_ANT	34 40
2228	RF_50S	50_RF_CLEAR	50_B1_B4_ANT_PHASESHIFT	34
595	RF_50S	50_RF_CLEAR	50_B2_TX_PAD_IN	35
594	RF_50S	50_RF_CLEAR	50_B3_TX_PAD_IN	35
591	RF_50S	50_RF_CLEAR	50_B2_DUPLX_RX	32 35
592	RF_50S	50_RF_CLEAR	50_B3_DUPLX_RX	32 35
597	RF_50S	50_RF_CLEAR	50_B2_DPLX_ANT	35
593	RF_50S	50_RF_CLEAR	50_B3_DPLX_ANT	35
2105	RF_50S	50_RF_CLEAR	50_B2_ANT	35 40
596	RF_50S	50_RF_CLEAR	50_B3_ANT	35 40
598	RF_50S	50_RF_CLEAR	50_B2_RX_BALUN	32
599	RF_50S	50_RF_CLEAR	50_B3_RX_BALUN	32
2226	RF_50S	50_RF_CLEAR	50_B2_ANT_PHASESHIFT	35
2227	RF_50S	50_RF_CLEAR	50_B3_ANT_PHASESHIFT	35
606	RF_50S	50_RF_CLEAR	50_B20_TX_PAD_IN	36
607	RF_50S	50_RF_CLEAR	50_B20_DPLX_ANT	36
605	RF_50S	50_RF_CLEAR	50_B20_ANT	36 40
2229	RF_50S	50_RF_CLEAR	50_B20_ANT_PHASESHIFT	
2107	RF_50S	50_RF_CLEAR	50_B5_TX_PAD_IN	37
2101	RF_50S	50_RF_CLEAR	50_B8_TX_PAD_IN	37
2104	RF_50S	50_RF_CLEAR	50_B5_DPLX_ANT	37
2103	RF_50S	50_RF_CLEAR	50_B8_DPLX_ANT	37
2105	RF_50S	50_RF_CLEAR	50_B5_ANT	37 40
2102	RF_50S	50_RF_CLEAR	50_B8_ANT	37 40
2224	RF_50S	50_RF_CLEAR	50_B5_ANT_PHASESHIFT	
2231	RF_50S	50_RF_CLEAR	50_B8_ANT_PHASESHIFT	37
2253	RF_50S	50_RF_CLEAR	50_B7_ANT	36 40
2254	RF_50S	50_RF_CLEAR	50_B7_BALUN_IN_RX	
2255	RF_50S	50_RF_CLEAR	50_B7_DPLX_ANT	36
2256	RF_50S	50_RF_CLEAR	50_B7_DUPLX_RX	32 36
2257	RF_50S	50_RF_CLEAR	50_B7_TX_PAD_IN	36
2258	RF_50S	50_RF_CLEAR	50_B7_TX_SAW_IN	36
2259	RF_50S	50_RF_CLEAR	50_B7_TX_SAW_OUT	36
2262	RF_50S	50_RF_CLEAR	50_XCVR_B7_TX	30 36
2123	RF_50S	50_RF_CLEAR	50_B13_TX_PAD_IN	38
2124	RF_50S	50_RF_CLEAR	50_B17_TX_PAD_IN	38
2126	RF_50S	50_RF_CLEAR	50_B13_DPLX_ANT	38
2125	RF_50S	50_RF_CLEAR	50_B17_DPLX_ANT	38
2127	RF_50S	50_RF_CLEAR	50_B13_LPF_IN	38
2130	RF_50S	50_RF_CLEAR	50_B13_ANT	38 40
2129	RF_50S	50_RF_CLEAR	50_B17_ANT	38 40
2232	RF_50S	50_RF_CLEAR	50_B13_ANT_PHASESHIFT	
2233	RF_50S	50_RF_CLEAR	50_B17_ANT_PHASESHIFT	38
2135	RF_50S	50_RF_CLEAR	50_XCVR_2G_LB_TX_MATCH	
2134	RF_50S	50_RF_CLEAR	50_XCVR_2G_HB_TX_MATCH	40
2132	RF_50S	50_RF_CLEAR	50_2G_LB_PA_IN	40
2133	RF_50S	50_RF_CLEAR	50_2G_HB_PA_IN	40
2225	RF_50S	50_RF_CLEAR	50_PRI_ANT_ASM	40
2145	RF_50S	50_RF_CLEAR	50_DRX_ANT_TEST	41 43
2221	RF_50S	50_RF_CLEAR	50_DRX_ANT_PHASESHIFT	43
2222	RF_50S	50_RF_CLEAR	50_DRX_ANT_FEED	43
2157	RF_50S	50_RF_CLEAR	50_COUPLER_TERM	
2156	RF_50S	50_RF_CLEAR	50_DIVERSITY_SWITCH_MATCH	41
2159	RF_50S	50_RF_CLEAR	50_GPS_LNA_OUT	41 42
2158	RF_50S	50_RF_CLEAR	50_GPS_ANT_COAX	42
2160	RF_50S	50_RF_CLEAR	50_GPS_ANT_MATCH	
2162	RF_50S	50_RF_CLEAR	50_GPS_ANT_TEST	
2220	RF_50S	50_RF_CLEAR	50_GPS_LNA_IN	42
2260	RF_50S	50_RF_CLEAR	50_PRI-ANT_COUPLER	
2261	RF_50S	50_RF_CLEAR	50_PRI-ANT_PHASE	
2240	RF_50S	50_RF_CLEAR	50_PRI_ANT_TEST	
2239	RF_50S	50_RF_CLEAR	50_PRI_ANT_TEST_IN	
2238	RF_50S	50_RF_CLEAR	50_PRI_ANT_COAX	40 43
2236	RF_50S	50_RF_CLEAR	50_ANT2_TERM	
2235	RF_50S	50_RF_CLEAR	50_DRX_ANT_TERM	
2237	RF_60		2G_FEM_S0	29 40
2238	RF_60		2G_FEM_S1	25 29 40
2239	RF_60		2G_FEM_S2	29 33 40
2240	RF_60		2G_FEM_S3	29 33 40
2241	RF_60		2G_FEM_S4	25 29 40
2242	RF_60		2G_FEM_S5	29 40
2243	RF_60		2G_FEM_S6	29 40
2244	RF_60		BB_PDM	29 39
2245	RF_60		BB_PDM_FILT	39
2246	RF_60		DCDC_ADJ	39
2247	RF_60		PA_R1	29 34 35 36 37 38

	NET_TYPE PHYSICAL	SPACING		
1279	RF_60		WTR_GP_DATA0	29 30
1278	RF_60		WTR_GP_DATA1	29 30
1277	RF_60		BB_ERROR_FLAG	25 29
1276	RF_60		PA_ON_B1_B4	29 34
1275	RF_60		PA_ON_B2_B3	29 35
1274	RF_60		PA_ON_B5_B8	29 37
1273	RF_60		PA_ON_B7_B20	29 36
1272	RF_60		PA_ON_B13_B17	29 38
1281	RF_60		PA_BS	29 34 35 36 37 38
1280	RF_60		LAT_SW1_CTL	25 29
1285	RF_60		PS_HOLD	27 29
1284	RF_60		WTR_RF_ON	25 29 30
1283	RF_60		WTR_RX_ON	25 29 30
1282	RF_60		DCDC_MODE	29 39
1281	RF_60		DCDC_ENABLE	
1286	RF_60		DRX_ASM_V1	29 41
1287	RF_60		DRX_ASM_V2	29 41
1285	RF_60		DRX_ASM_V3	29 41
1284	RF_60		DRX_ASM_V4	29 41
1290	RF_60		19P2M_CLK_EN	27 28
1289	RF_60		PMIC_RESOUT_L	25 27 28
1288	RF_60		PMIC_SSBI	25 27 28

	NET_TYPE PHYSICAL	SPACING		
1107	RF_DIFF	RF_DIFF	RF_60	TX_BB_Q_P 29 30
1109	RF_DIFF	RF_DIFF	RF_60	TX_BB_Q_N 29 30
1108	RF_DIFF	RF_DIFF	RF_60	DRX_BB_Q_P 29 30
1110	RF_DIFF	RF_DIFF	RF_60	DRX_BB_Q_N 29 30
1112	RF_DIFF	RF_DIFF	RF_60	GPS_BB_Q_P 29 30
1111	RF_DIFF	RF_DIFF	RF_60	GPS_BB_Q_N 29 30
1113	RF_DIFF	RF_DIFF	RF_60	PRX_BB_Q_P 29 30
1114	RF_DIFF	RF_DIFF	RF_60	PRX_BB_Q_N 29 30
1115	RF_DIFF	RF_DIFF	RF_60	DRX_BB_I_P 29 30
1116	RF_DIFF	RF_DIFF	RF_60	DRX_BB_I_N 29 30
1117	RF_DIFF	RF_DIFF	RF_60	GPS_BB_I_P 29 30
1118	RF_DIFF	RF_DIFF	RF_60	GPS_BB_I_N 29 30
1119	RF_DIFF	RF_DIFF	RF_60	PRX_BB_I_P 29 30
1120	RF_DIFF	RF_DIFF	RF_60	PRX_BB_I_N 29 30
1122	RF_DIFF	RF_DIFF	RF_60	TX_BB_I_P 29 30
1121	RF_DIFF	RF_DIFF	RF_60	TX_BB_I_N 29 30
1169	RF_DIFF	RF_100D	100_RF	100_XCVR_B13_B17_B20_PRX_P 30 33
1170	RF_DIFF	RF_100D	100_RF	100_XCVR_B13_B17_B20_PRX_N 30 33
1171	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_PRX_P 30 32
1172	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_PRX_N 30 32
1173	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_PRX_P 30 32
1174	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_PRX_N 30 32
1175	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_PRX_P 30 32
1176	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_PRX_N 30 32
1177	RF_DIFF	RF_100D	100_RF	100_XCVR_B3_PRX_P 30 32
1178	RF_DIFF	RF_100D	100_RF	100_XCVR_B3_PRX_N 30 32
1179	RF_DIFF	RF_100D	100_RF	100_XCVR_DCS_PCS_PRX_P
1181	RF_DIFF	RF_100D	100_RF	100_XCVR_DCS_PCS_PRX_N
1182	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_PRX_P 30 32
1180	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_PRX_N 30 32
1184	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_B20_DRX_P 30 41
1183	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_B20_DRX_N 30 41
1185	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_B13_B17_DRX_P 30 41
1187	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_B13_B17_DRX_N 30 41
1186	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_B3_DRX_P 30 41
1189	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_B3_DRX_N 30 41
1190	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_DRX_P 30 41
1188	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_DRX_N 30 41
1192	RF_DIFF	RF_100D	100_RF	100_XCVR_GPS_RX_P 30 41
1191	RF_DIFF	RF_100D	100_RF	100_XCVR_GPS_RX_N 30 41
1195	RF_DIFF	RF_100D	100_RF	100_B13_DUPLX_RX_P 32 38
1193	RF_DIFF	RF_100D	100_RF	100_B13_DUPLX_RX_N 32 38
1194	RF_DIFF	RF_100D	100_RF	100_B17_DUPLX_RX_P 32 38
1197	RF_DIFF	RF_100D	100_RF	100_B17_DUPLX_RX_N 32 38
1196	RF_DIFF	RF_100D	100_RF	100_B20_DUPLX_RX_P 32 36
1199	RF_DIFF	RF_100D	100_RF	100_B20_DUPLX_RX_N 32 36
1198	RF_DIFF	RF_100D	100_RF	100_DCS_PCS_RX_FILTER_P
1200	RF_DIFF	RF_100D	100_RF	100_DCS_PCS_RX_FILTER_N
1205	RF_DIFF	RF_100D	100_RF	100_B1_B4_DUPLX_RX_P 32 34
1206	RF_DIFF	RF_100D	100_RF	100_B1_B4_DUPLX_RX_N 32 34
1207	RF_DIFF	RF_100D	100_RF	100_B8_DUPLX_RX_P 32 37
1210	RF_DIFF	RF_100D	100_RF	100_B8_DUPLX_RX_N 32 37
1211	RF_DIFF	RF_100D	100_RF	100_B5_B18_DUPLX_RX_P 32 37
1209	RF_DIFF	RF_100D	100_RF	100_B5_B18_DUPLX_RX_N 32 37
1165	RF_DIFF	RF_100D	100_RF	100_B7_PRX_BALUN_OUT_P 32
1164	RF_DIFF	RF_100D	100_RF	100_B7_PRX_BALUN_OUT_N 32
1163	RF_DIFF	RF_100D	100_RF	100_B7_PRX_MATCH_P 32
1167	RF_DIFF	RF_100D	100_RF	100_B7_PRX_MATCH_N 32
1208	RF_DIFF	RF_100D	100_RF	100_XCVR_B7_PRX_P 30 32
1166	RF_DIFF	RF_100D	100_RF	100_XCVR_B7_PRX_N 30 32
1349			RF_CLK	SLEEP_CLK_32K 25 27 28
1352			RF_CLK	19P2M_WTR 27 30
1353			RF_CLK	19P2M_MDM 25 27 28

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50_RF_SPACING	TOP,BOTTOM	0.178 MM	?
50_RF_SPACING	ISL3	0.130 MM	?
50_RF_SPACING	*	0.092 MM	?
50_RF_CLEAR_SPACING	TOP,BOTTOM	0.178 MM	?
50_RF_CLEAR_SPACING	ISL3	0.130 MM	?
50_RF_CLEAR_SPACING	*	0.138 MM	?
100_RF_CLEAR_SPACING	TOP,BOTTOM	0.143 MM	?
100_RF_CLEAR_SPACING	*	0.118 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	50_RF	*	50_RF_CLEAR_SPACING
GND	50_RF_CLEAR	*	50_RF_CLEAR_SPACING
GND	100_RF	*	100_RF_CLEAR_SPACING
GND	RF_60	*	1.2:1_SPACING
GND	PWR_RF	*	1.2:1_SPACING
PWR_RF	PWR_RF	*	1.2:1_SPACING
RF_CLK	*	*	3:1_SPACING
RF_CLK	GND	*	1.2:1_SPACING

NC_PMU_OUT_32K_CLK_GPS == PMU_OUT_32K_CLK_GPS
NO_TEST=TRUE
MAKE_BASE=TRUE
IN 57 64

RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	50_OHM_RF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
WIFI	*	*	4:1_SPACING